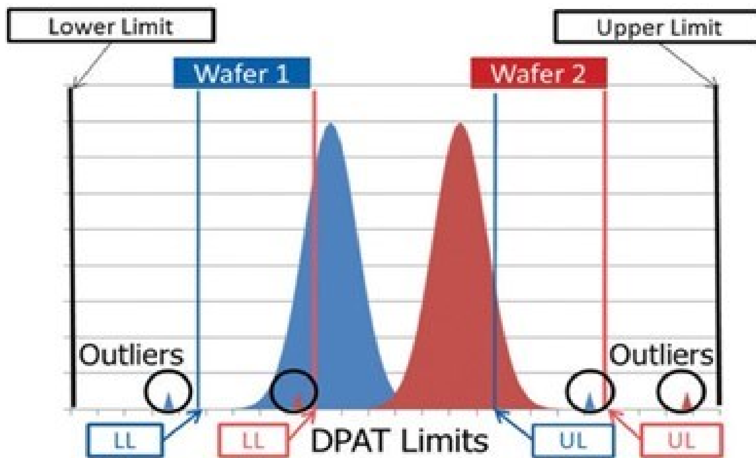
Intelligent Outlier Detection & Removal for Semiconductor Devices

Galaxy PAT-Man

DATASHEET



PAT-Man, with hundreds of billions of devices processed worldwide, excels in detecting and excluding outlier devices that could compromise long-term reliability. It balances defects per million (DPM) and yield, integrating seamlessly with existing test environments to deliver industry-leading DPM reduction.

PAT-Man includes a powerful recipe editor and yield simulator that enables users to experiment with different tests and PAT algorithms while measuring the resulting yield impact based on simulations from historical data.

Recipes can be based on a combination of spatial patterns like GDBN (good die in bad neighborhood), industry standards like SYA (AEC-Q002 compliant statistical yield analysis), or even Galaxy's proprietary "Smart & Adaptive" analysis system which employs sophisticated shape detection algorithms that automatically adjust for gaussian and many non-gaussian distributions on-the-fly. PAT-Man also incorporates site specific limits to compensate for tester, probe card, and socket variations and drifts, thereby eliminating unnecessary yield loss.

Pat-Man offers industry leading algorithms including multi-variate PAT (MV-PAT) which evaluates all test results simultaneously instead of looking at each test individually, containing outliers that other recipes miss while minimizing incremental yield cost.

PAT-Man is a scalable solution whether at a pre-revenue startup with one engineer, a global company with thousands of engineers, or anywhere in between. For those with smaller volumes who need the flexibility of the recipe generator but may not currently need the automation engine of the full PAT-Man solution, ask us about PAT-Man Lite!

For more than 25 years Galaxy Semiconductor is the trusted solution for enhancing yields, reducing defects per million (DPM), and optimizing semiconductor manufacturing processes. Galaxy's experienced team provides powerful, scalable, and easy to use intelligent data analytics while providing first class support.

FEATURES AND BENEFITS

- Automated outlier removal for wafer sort and final test.
- Supports SPAT, DPAT, Z-PAT, Multi-Variate PAT, GDBN, Clustering, NNR, reticle patterns, automatic scratch detection and custom recipes
- Smart & Adaptive recipes with automatic shape detection:
  – Gaussian
  – Gaussian with one tail (L or R)
  – Gaussian with two tails
  – LogNormal (L or R tail)
  – Multi-modal
  – Bimodal
  – Clamped (one side)
  – Clamped (two sides)
  – Categorical (distinct classes)
- Easy to use recipe editor with automated test selector and yield impact simulator
- Automatic evaluation of parametric results to determine PAT eligibility.
- Yield-Man integration for AEC-Q002 compliant Statistical Yield Analysis and maverick lot detection
- PAT and raw binning automatically stored in relational database
- Special PAT reports, including:
  – PAT bin Pareto
  – PAT yield trend
  – Rule effectiveness
  – Tests with most outliers
  – Marginal dies
- PAT yield alarms – Low yield alert
- Integrates with MES systems for fully automated operation

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