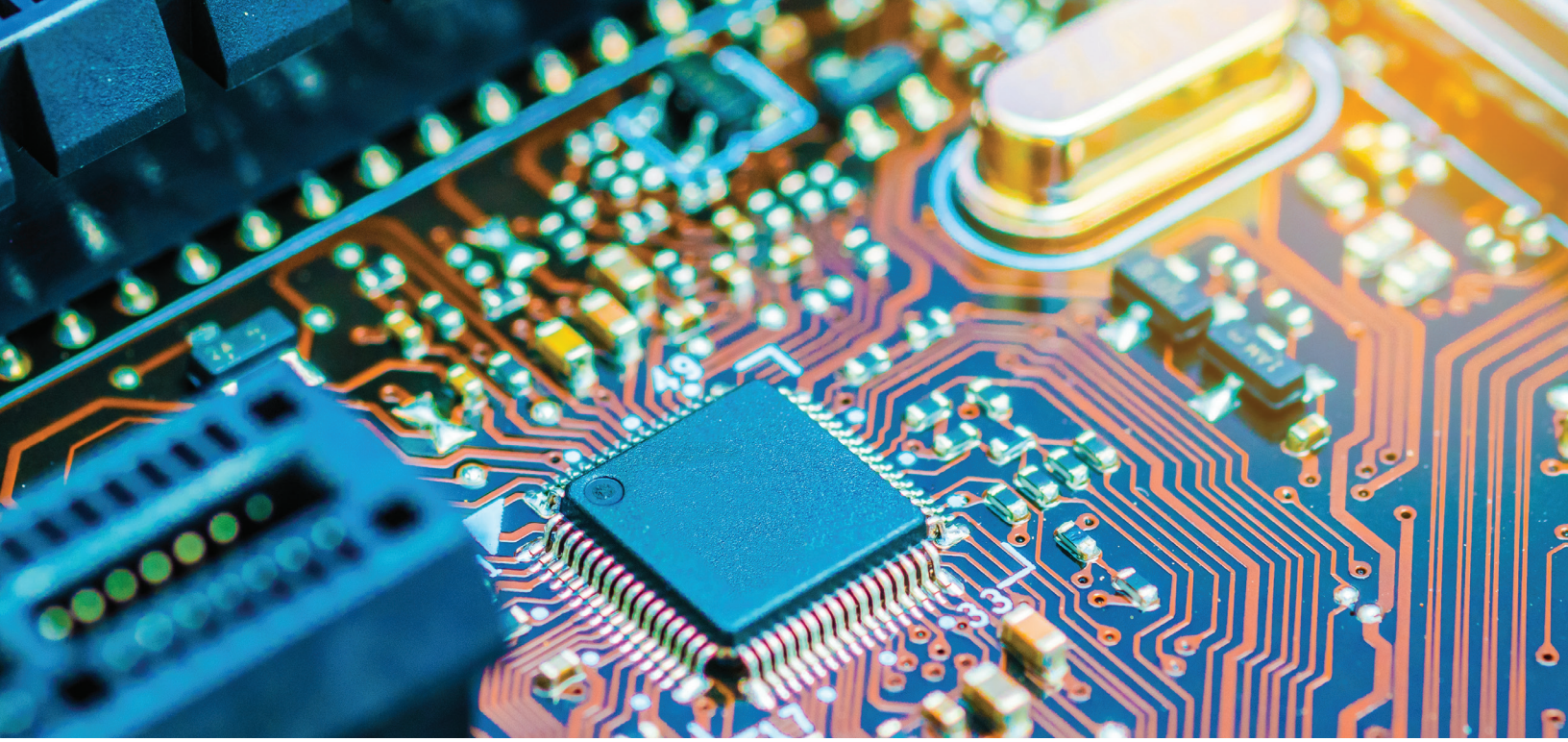


DIGITAL INDUSTRIES SOFTWARE

Solido FastSPICE

Accelerated FastSPICE simulation for SoC and memory designs

Features and benefits

Order-of-magnitude speedup with equal or better accuracy versus other fast SPICE simulators

- Unified use model for SPICE to Fast SPICE scaling
- Tunable partition and multi-rate simulation
- High-performance and accurate SPS (Single Partition Solver) based on the AFS engine
- Advanced parasitic reduction modes for the highest performance

Multi-resolution measurement-aware technology

- Full measurements and waveforms with high resolution for critical paths

Modern trends in chip designs, propelled by advancements such as advanced-node adoptions and "More than Moore" designs, have significantly increased design complexity. As analog and custom IC designers strive to meet these demands, they encounter formidable obstacles in the form of slow and lengthy simulations that often fail to adequately cover all aspects of verification. The Siemens EDA Solido FastSPICE simulator uniquely delivers.

Solido™ FastSPICE, with multi-resolution technology, is a next-generation fast SPICE simulation tool with scalable accuracy for analog and mixed-signal transistor-level functional verification and memory/analog characterization. It features a unified model for SPICE and Fast SPICE scaling, tunable partitioning, topology/circuit-based detection, multi-rate simulation, table-based device modeling, measurement aware simulation technology, and advanced parasitic reduction modes for the highest performance.

The combined technologies provide circuit designers with a unified simulation interface to achieve simulation results order-of-magnitude faster than traditional SPICE simulation with predictable accuracy. Solido FastSPICE supports industry-standard netlist formats and is integrated into the Symphony™ mixed-signal simulation solution, supporting full-chip SoC verification.

Features and benefits

continued

Intuitive use model and debug

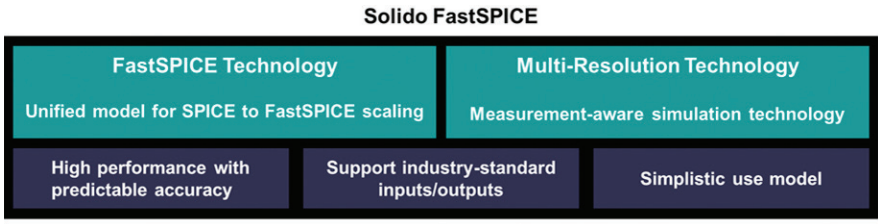
- Out-of-the-box or single command settings
- Accuracy versus performance tuning through preset simulation modes
- Save-restore for improved productivity

Supported analyses

- DC and transient analyses

Support of industry standard SPICE flows

- Supports industry standard netlist formats, outputs, and simulation models
- Tight integration with Symphony™ mixed signal simulator platform



Analog and Mixed-Signal Transistor-Level Functional Verification
Memory/Analog Characterization

Solido FastSPICE key functionality:

- Order-of-magnitude faster than traditional fast SPICE
- Equal or better accuracy than traditional fast SPICE
- Capacity to handle memories and SoCs with post-layout parasitics
- DC and Transient analyses
- Tunable partitioning algorithm
- Table-based device modeling
- Advanced parasitic reduction modes
- Measurement-aware technology
- Mixed-signal SoC verification through integration with Symphony simulator

Solido FastSPICE specifications:

Input formats:

- SPICE netlist formats
- Verilog-A
- DSPF, SPF, and DPF
- Digital Vector and VCD files

Output waveform formats:

- FSDB
- WDB
- PSF

Analyses:

- DC
- Transient

Device models:

- Same as supported by Analog FastSPICE

Solido FastSPICE support:

- Standalone command line
- Leading EDA design environment
- Commercially available cloud offerings

Hardware Requirements:

- Single-core or multi-core systems
- x86 architecture
- Operating System: Linux

Siemens Digital Industries Software

siemens.com/software

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1 800 498 5351

Europe
00 800 70002222

Asia-Pacific
001 800 03061910

For additional numbers, click here.

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