



## DIGITAL INDUSTRIES SOFTWARE

# Solido LibSPICE

Accelerated SPICE simulation for batch verification of library IP designs

### Features and benefits

#### High accuracy, high performance for small designs

- Performance acceleration up to 15X for standard cell and memory bit-cell verification
- New solver optimized for small designs with <10k elements
- Single threaded with multi-core parallel support

#### Native integration with Solido™ Design Environment for batch verification flows

Native integration with Solido™ Characterization Suite for batch flows with Solido library characterization technology

### Introduction

Solido LibSPICE is Siemens' purpose-built batch solver technology for small designs, providing up to 15X speedups for library IP applications. Solido LibSPICE is natively integrated into Siemens' Solido Design Environment and Solido Characterization Suite for performance acceleration, enabling a full-flow solution for robust verification of standard cells and memory bit-cells. It supports Eldo, HSPICE, and Spectre netlist formats.

Solido LibSPICE		
<b>High accuracy, high performance for small designs</b> SPICE-accurate simulator purpose built with advanced device model evaluation and matrix solve	<b>Integrated with Solido Design environment and library yield solver</b> Maximizes re-use across batches of short simulations	<b>Integrated with Solido Characterization Suite</b> High performance library IP characterization for .lib generation
Command line accessible for acceleration with Solido Sim AI	SPICE syntax-agnostic Supports industry-standard outputs	Ideal for Batch flows – statistical, sweeps

**Features and benefits***continued***Fastest variation-aware design and verification**

- SPICE accurate, 1,000x faster than brute force simulation
- Accelerated high-sigma verification with Solido Sim AI technology

Key benefits for Solido LibSPICE are:

- New solver optimized for small designs
- Maximizes re-use across batches of short simulations
- Natively integrated with Solido Design Environment and Solido Characterization Suite
- Optimized for batch simulation flows, including statistical, alters and sweeps

**Specifications****Analyses**

- DC, Transient
- Alter, Sweep, Monte Carlo

**Input/Output formats**

- HSPICE, Spectre, Eldo netlist syntax
- DSPF back-annotation
- VCD, .vec
- FSDB, tr0, PSF, Nutmeg, WDB

**Integrated with Solido Design Environment**

- Batch verification capability for library IP verification
- Optimized for Library Yield Solver flows

**Integrated with Solido Characterization Suite**

- Batch verification capability for library characterization

**Other support**

- Invocation via Command line and Solido Design Environment
- Supported with commercially available cloud offerings

**Device models**

- BSIM3/4/6, BSIMSOI, BSIM-CMG, BSIM-IMG, BSIMSOI, MOS11, PSP, EKV, HiSIM2, HiSIM-SOI, HiSIM\_HV, GaN ASM, GaN MVSG
- MOS1/3, MOSVAR, JFET, Diode, Juncap
- UTSOI, L-UTSOI, MM20, VBIC, Simkit
- Interface, BJT, HICUM, Mextram, Gummel-Poon, S-parameter, W element, bsource, Verilog-A, Verilog-AMS

**Hardware requirements**

- Single-core or multi-core systems
- Minimum memory recommendation: For installation: 3 GB of disk space
- For simulation: 2 GB of physical memory (RAM) and 2 GB of swap space (virtual memory)
- Operating System: Linux® RHEL7+ SLES12+

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