



DIGITAL INDUSTRIES SOFTWARE

Solido SPICE

Accelerated SPICE simulation for next-generation AMS, RF, memory, and 3D IC designs

Features and benefits

Fastest nanometer-accurate SPICE Simulation

- Certified by leading foundries
- Up to 30X faster than accelerated SPICE simulators for large designs
- New solver technology for large pre- and post-layout designs, cache-efficient
- Advanced parasitic reduction technologies for post-layout designs, including a new high-performance mode compared to AFS
- 500M-element capacity

Introduction

Solido™ SPICE is the next-generation, feature-rich, high-capacity and SPICE-accurate simulation technology, providing 2-30X speedup for analog, mixed-signal, RF, memory, custom digital, and library IP applications, with foundry certified accuracy.

Solido SPICE includes all capabilities of Analog FastSPICE (AFS), and in addition, has many new verification technologies.

Solido SPICE		
<p>High accuracy, high performance for large pre- and post- layouts</p> <p>SPICE simulator with next-gen matrix solver, new parasitic reduction and complex S-parameter handling</p>	<p>Full-spectrum and multi-tone analyses</p> <p>Production-tested transient noise, RF shooting newton & harmonic balance for RFIC design</p>	<p>Multi-die and 3D IC verification enabled</p> <p>Best-in-class high-speed interface verification with equalization, and multi-technology support</p>
<p>Foundry-certified PDKs</p>	<p>SPICE syntax-agnostic</p> <p>Supports industry-standard outputs</p>	<p>Supports all Custom IC SPICE flows</p> <p>High-sigma variation, characterization, mixed signal, analog fault, EM/IR, PERC</p>

Features and benefits *continued*

New advanced RF analyses for circuits driven by digital RF modulation schemes

New advanced high-speed link verification technology

for SPICE-accurate TX-to-RX transient analysis, including equalization

Fastest full-spectrum and multi-tone analyses

- Includes all device noise sidebands/ harmonics
- Transient noise within 1 to 2 dB of silicon data
- Shooting Newton (PSS) and harmonic balance large and small signal analyses

Input/Output formats

- DSPF back-annotation
- VCD, .vec
- FSDB, tr0, PSF, Nutmeg, WDB
- HSPICE, Spectre, Eldo syntax compatibility

New performance technologies

Solido™ SPICE has a new scalable and cache-efficient solver, which provides a significant performance boost for large pre- or post-layout designs. Solido SPICE is also engineered with new and advanced parasitic reduction technology. In combination, these technologies enable designers to handle larger and fully RC extracted designs.

New advanced RF verification technology

Solido SPICE supports RF classic and fast-envelope analyses for verifying advanced digital RF communication designs. It applies for circuits operating with complex I/Q limited-bandwidth waveforms, commonly found in digital modulation schemes. Solido SPICE supports various wireless modulation standards, such as 802.11ax, 802.11n etc., enabling critical measurements like constellation diagrams, error vector magnitude (EVM), and power spectral density (PSD). These simulation capabilities are crucial for predicting nonlinear distortion effects in circuits like power amplifiers (PAs), oscillators and RF modules used in Wi-Fi applications.

New advanced high-speed link verification technology

In-die, multi-die, 3D IC and memory interface developers can now experience an efficient capability for high-speed link verification including equalization, without breaking up the transmission through receive paths into different cross-sections. Solido SPICE enables the simulation of netlists with SPICE models, S-parameters, IBIS models and IBIS-AMI algorithmic models to capture die, package, and board-level effects for accurate signal integrity analysis. This enables high-accuracy time-domain waveform processing of channel losses, circuit nonlinearities, and equalization effects, resulting in accurate and accelerated verification of transmission for SERDES and DDR applications.

Siemens solution flows

Solido SPICE supports Eldo, HSPICE, and Spectre netlist formats and is integrated into the Symphony™ mixed-signal simulation solution, supporting AoT and DoT verification flows. Solido SPICE is natively integrated within Siemens AI-powered Solido™ Design Environment for variation-aware verification and Solido™ Characterization Suite for .lib generation, enabling customers to execute IC signoff flows with superior performance, high accuracy, and scalability across cloud infrastructure. Further, Solido SPICE powers Siemens IC sign-off flows with Calibre® Design solutions, Tessent™ silicon lifecycle management solutions as well as Siemens' Electronic Board Systems solutions, providing full-flow verification solutions across applications.

Solido SPICE specifications

Analyses

- DC
- Transient
- Alter
- Sweep
- Monte Carlo
- Transient noise analysis
 - Full-spectrum accuracy to noise floor
 - Device noise analysis for any circuit type
 - Same element capacity as transient
 - Validated to within 1 to 2 dB of silicon
- RF Analyses
 - Shooting Newton (SN) and Harmonic Balance (HB) analyses
 - PSS SN - pac/pxf/pnoise/pstb/psp Full-Spectrum periodic noise and oscillator noise
 - Single-tone PSS, sampled and modulated pnoise, sampled pac and pxf
 - > 3M element PSS convergence, no maxsideband
 - HB - hbac/hbxf/hbnoise/hbstb/hbsp Multi-Tone HB and modulated hbnoise
- > 6M element HB convergence

Input/Output formats

- DSPF back-annotation
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- FSDB, tr0, PSF, Nutmeg, WDB

Solido SPICE powers Siemens EDA signoff IC flows

- Variation-aware verification with the **Solido™ Design Environment**
- Library characterization with the **Solido™ Characterization Suite**
- Mixed-signal verification with **Symphony**

- Waveform viewing and customized post-processing with **Solido Waveform Analyzer**
- Context-aware ESD Simulation with **Calibre® PERC™**
- EM/IR Simulation with **mPower™** for power and signal reliability
- Transistor-level fault simulation with **Tessent DefectSim** for analog defects
- Library creation for cell-aware ATPG & scan-based diagnosis with **Tessent CellModelGen**
- Electro-thermal analysis with **Calibre® 3DThermal** for 3D IC design flows
- Advanced IO verification with **HyperLynx™** for signal integrity

Device models

- BSIM3/4/6, BSIMSOI, BSIM-CMG, BSIM-IMG, BSIMSOI, MOS11, PSP, EKV, HiSIM2, HiSIM-SOI, HiSIM_HV, GaN ASM, GaN MVSG
- MOS1/3, MOSVAR, JFET, Diode, Juncap
- UTSOI, L-UTSOI, MM20, VBIC, Simkit
- Interface, BJT, HICUM, Mextram, Gummel-Poon, S-parameter, W element, bsource, Verilog-A, Verilog-AMS

Other support

- Invocation via command line and leading EDA design environments
- Supported with commercially available cloud offerings

Hardware requirements

- Single-core or multi-core systems
- Minimum memory recommendation: For installation: 3 GB of disk space
- For simulation: 2 GB of physical memory (RAM) and 2 GB of swap space (virtual memory)
- Operating System: Linux® RHEL7+ SLES12+

Siemens Digital Industries Software siemens.com/software

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