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Using Calibre eqDRC design rule checking for curved layouts in silicon photonics

Executive summary

Silicon photonics integrated circuit components include unconventional geometries, such as curvilinear (non-Manhattan) shapes. Calibre eqDRC technology enables designers to verify such components by applying multi-dimensional tolerance checking and using rule-based equations that model the behavior of the complex typical structures. With the accuracy of Calibre eqDRC verification, silicon photonics designers can enjoy more design freedom with confidence in the results.

Mohaned Elshawy

Introduction

Using Calibre eqDRC verification methodology for curved layouts in silicon photonics

Silicon photonics (SiP) integrated circuit (IC) components include unconventional geometries, such as curvilinear (non-Manhattan) shapes. Dealing with these shapes presents a challenge for traditional design rule checking (DRC) tools developed for Manhattan shapes. Calibre® eqDRC technology handles such challenges by applying multi-dimensional tolerance checking and using rule-based equations that model the behavior of the complex typical structures for more accurate results. Two examples illustrate the problem and demonstrate how Calibre eqDRC functionality tackles these issues..

What's the problem?
Silicon photonics components are usually formed by curvilinear geometries (non-Manhattan shapes). Traditional IC DRC tools are incompatible with these geometries, resulting in false errors reported during the physical verification phase.

Potential impact?
Increased debug time due to false errors induced by irregular shapes.

Missed real errors associated with common photonic structures due to limited or one-dimensional checks.

Calibre Solution
Using Calibre eqDRC technology, design rules can be modeled in the form of equations. These new rules can properly identify real violations while filtering out unwanted false errors.

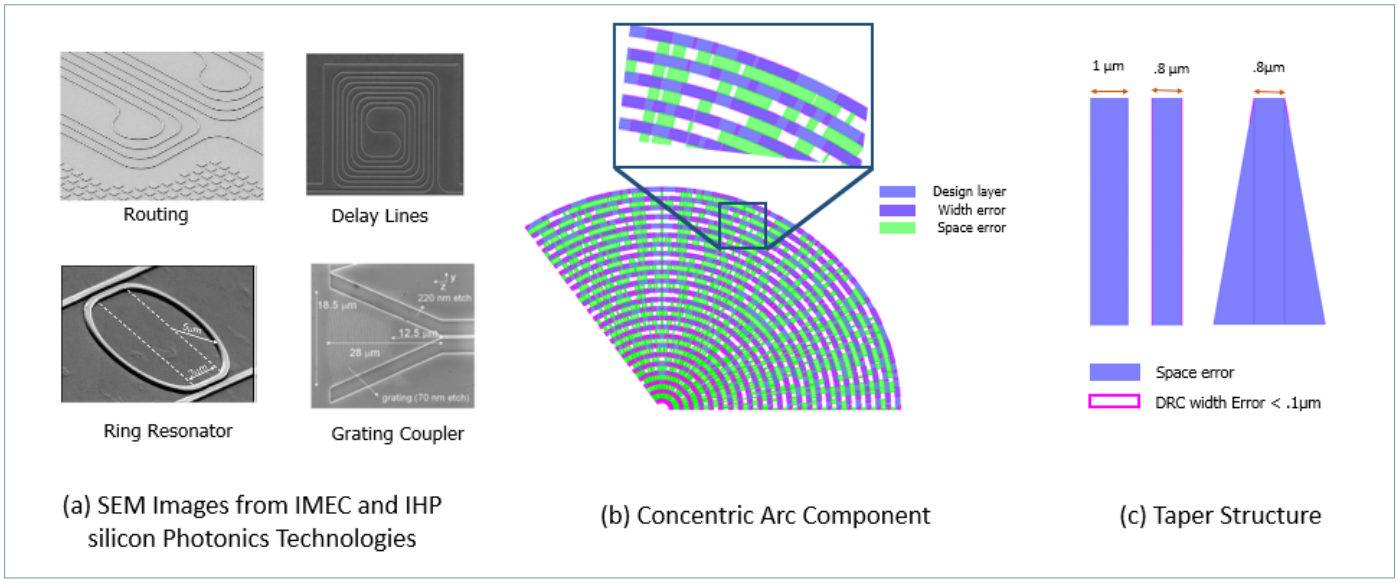

Figure 1: Silicon photonic components. (a) SEM images for SiP components (sources: IMEC and IHP); (b) Concentric arc layout with false DRC width and spacing violations; (c) Taper structure layouts with different widths..

DRC challenges in photonics designs

Traditional DRC tools ensure that the geometric layout of a design follows the foundry's prescribed rules to achieve acceptable yield. Traditional CMOS devices, as represented in a GDSII or OASIS database, are described as a set of coordinates that form a polygon as a closed loop of straight lines (Manhatttan shapes), snapped to a specific technology grid. SiP components, like those shown in figure 1a, introduce new geometric challenges. Most of these shapes, such as curves, spikes, and tapers, are curvilinear (non-Manhattan) shapes. To represent these shapes in the layout database, curves must be rendered into linear piecewise approximations, and all off-grid vertex coordinates snapped to nearest grid. This shift can range up to .5 DBU along the X-axis and Y-axis. When checking the dimensions of the curvilinear shapes, this grid snapping may cause the DRC engine to report thousands of unnecessary DRC violations (figure 1b).

Additionally, traditional one-dimensional rule checks are insufficient to perform accurate checking. Figure 1c shows different layouts for a typical taper structure with different widths. The traditional DRC engine may report width violations at the trapezoid end, although the technology allows width design freedom as long as the trapezoid angle is greater than a certain value (to ensure a robust structure for fabrication). Consequently, traditional DRC applications must be extended to handle these challenges.

Tackling photonics designs with Calibre eqDRC technology

With the Calibre eqDRC language, traditional DRC capability is extended to assist users in analyzing complex and multi-dimensional rules that are hard or impossible to implement with traditional methods. The rule writer has the ability to apply conditional DRC rules with multi-dimensional tolerance values to perform difficult checks on curvilinear shapes. Moreover, complex rules used for common structures can be modeled into equations to enable accurate results capture, without the inclusion of false errors.

Reducing false errors with conditional rules

To avoid the grid snapping effect for non-Manhattan shapes, rule writers can apply multi-dimensional tolerance factors that are based on the layout grid. These tolerance values can be used to filter out the false errors. For example, in traditional DRC, simple dimension rules may be described as follows:

$\text{Error\_rod\_width} \coloneqq \text{Width(rod)} < 1\mu m$

$\text{All\_Thin\_space} \coloneqq \text{Space(rod)} < 1\mu m$

where rod is the design layer for the concentric arcs. Such rules report thousands of false width and space violations, making it very difficult for a designer to discern real errors from false errors. A width or spacing measurement can vary up to $2\sqrt{2} \times$ (grid_size), or two times the diagonal distance of the square grid, due to a point on the curve being snapped to a layout grid. As a result, using a tolerance factor of 0.15 µm eliminates these false errors. By applying these tolerances only to results with a small displacement angle, and of sufficiently small lengths as compared to the overall curve structure, they can be tuned to the expected curvature as below:

$\text{All\_Thin\_rod} \coloneqq \text{Width(rod)} < 1\mu m$

$W = \text{Width(thin\_rod\_width)}$

$\alpha = \text{Angle(thin\_rod\_width)}$

$L = \text{Length(thin\_rod\_width)}$

if $\{(0<\alpha<5)$ or $(L<1)\}$ Then:

$\text{Error\_rod\_width} \coloneqq \text{Width(rod)} < 0.985\mu m$

Else:

$\text{Error\_rod\_width} \coloneqq \text{Width(rod)} < 1\mu m$

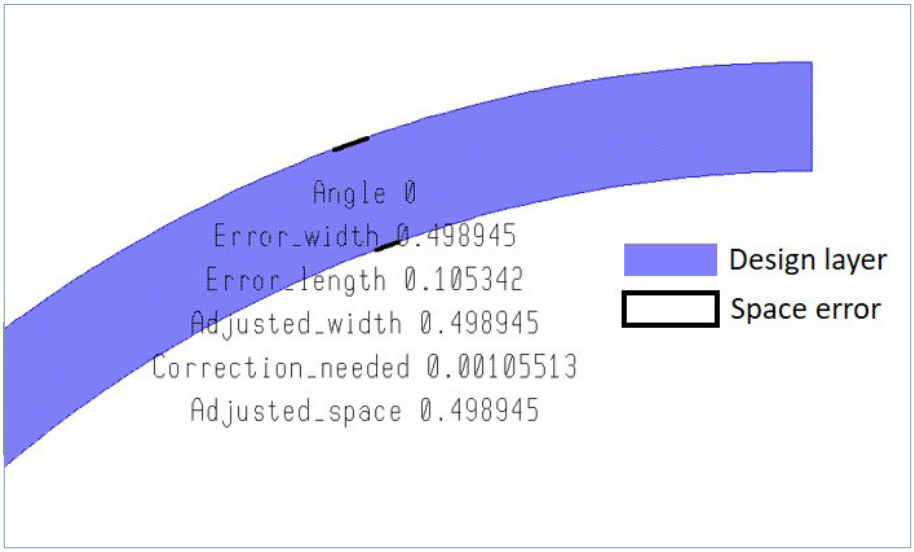

Figure 2: Visualizing error for ease of debugging.

The Angle operation detects the error edge pair with an angle between 0 and 5, representing the slight misalignment of the opposite edges of a grid-snapped geometry. The Length operation determines the error edges with lengths smaller than 1 µm, which is the small fractured segment of a much larger curve. After using this approach, unintended false errors are completely eliminated. The advantage of the conditional DRC tolerance application is that the user no longer needs to compromise the accuracy of the rest of the design due to the presence of the curvilinear shapes.

Visualizing error information

Unlike traditional DRC, which provides only pass and fail results, the Calibre eqDRC language facilitates debugging by annotating illegal designs with fully-customized error correction information. To visualize the error on the design, the rule writer must create the appropriate output properties by reverse-engineering the failure constraint to get the needed correction. Figure 2 shows a highlighted error on a pair of edges, with various customized parameters.

Enabling multi-dimensional checks

To allow a wider range of photonic design shapes in masks, as well as to solve the problem of distinguishing surface facets, a physical model with simultaneous constraints can be used (for example, applying width checking to a taper structure based on the geometric angle). Figure 3 shows a two-dimensional array of trapezoids. The width varies from 0.05µm to 1.05µm in the horizontal direction, and the angle varies from 0 to 90°.

The blue line is the curve representing the physical constraints that can be implemented closest to the extended fabrication constraint, which secures the maximum freedom in photonic layout design. Contrary to traditional 1D rules, the multi-dimensional Calibre eqDRC rule can be written to consider both width and angle dimensions related by the model:

$$\alpha = \mathrm{Angle(rod)}\ ,\ \alpha c = f(\mathrm{Width(rod)})$$

$$\mathrm{Then,\ Thin\_rod} = \alpha/\alpha c > 1$$

Conclusion

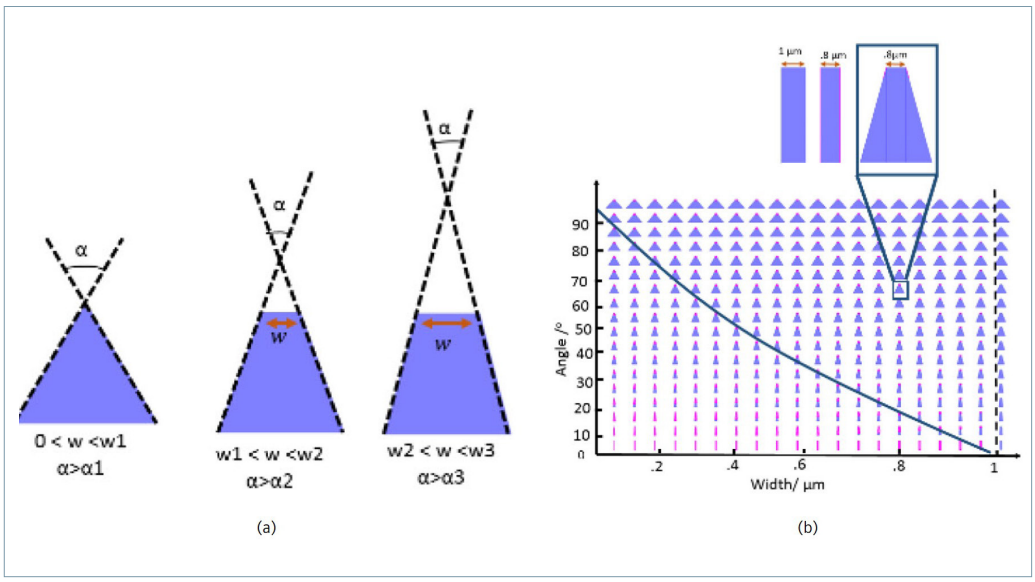

Figure 3: Taper structures layout with different widths and angles (a) Design rules: w is the width and α is the angle between two adjacent edges (b) Solid line and dashed line are the modeled and traditional rules respectively.

Where α is the measured value and α_c is the calculated critical angle given by the function (ƒ). As shown in Figure 3, only designs on the left side of the modeled rule (solid line) are reported as errors. The traditional DRC rule reports errors to all designs with width under 1 µm. Using the Calibre eqDRC rule means more design shapes are now accepted, since the rule is now modeled to describe the actual physical constraint. As a result, more freedom is allowed in the design while the accuracy is increased, which is required in photonic layout designs.

Siemens Digital Industries Software

Headquarters
Granite Park One
5800 Granite Parkway
Suite 600
Plano, TX 75024
USA
+1 972 987 3000

Americas
Granite Park One
5800 Granite Parkway
Suite 600
Plano, TX 75024
USA
+1 314 264 8499

Europe
Stephenson House
Sir William Siemens Square
Frimley, Camberley
Surrey, GU16 8QD
+44 (0) 1276 413200

Asia-Pacific
Unit 901-902, 9/F
Tower B, Manulife Financial Centre
223-231 Wai Yip Street, Kwun Tong
Kowloon, Hong Kong
+852 2230 3333

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