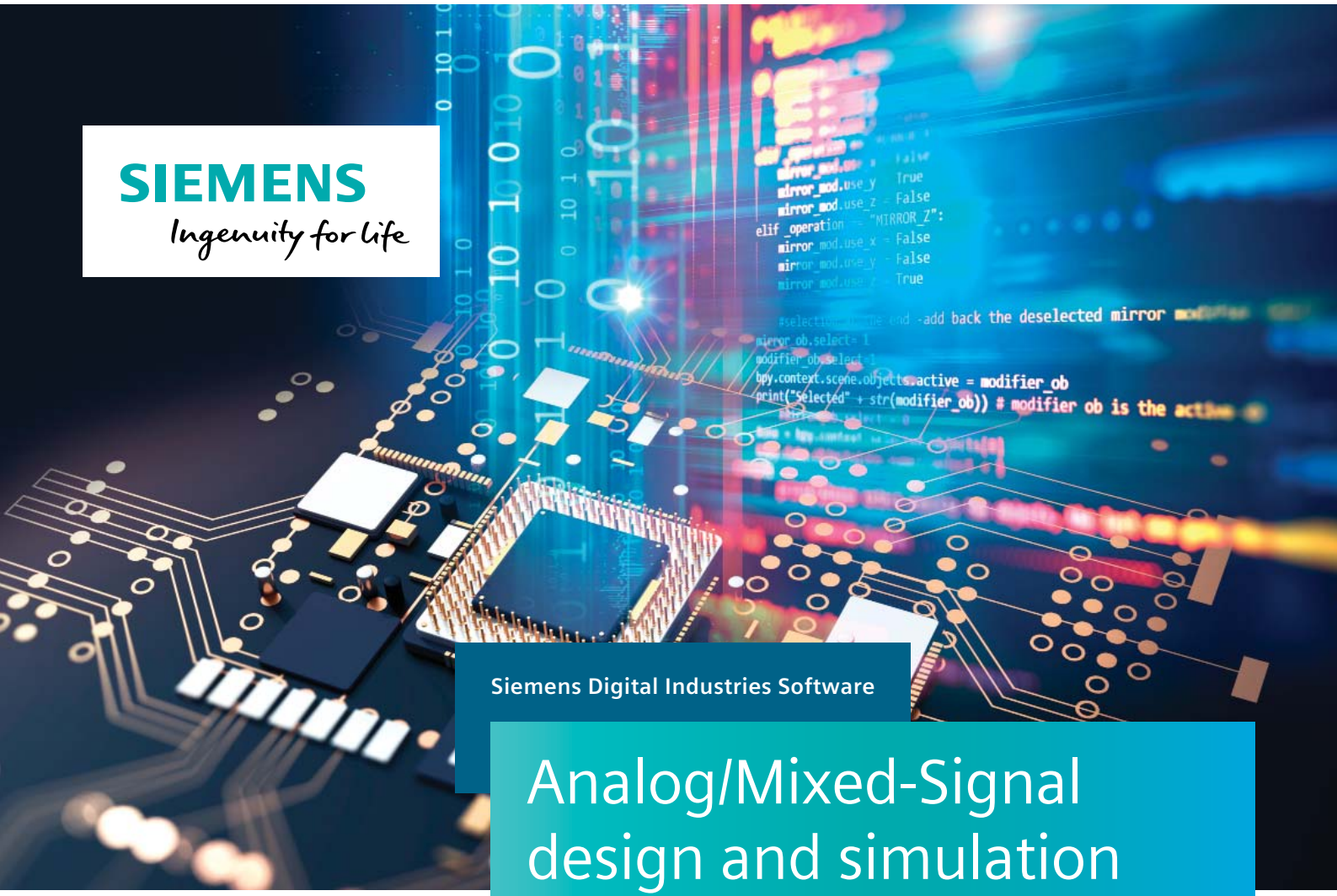

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Analog/Mixed-Signal design and simulation in a Tanner flow

Custom IC Design

Executive summary

The Tanner flow simplifies the design and verification process of Analog/Mixed-Signal design. The user can verify design functionality, connectivity and performance at all levels of the design hierarchy and for all integrated circuit (IC) applications.

Introduction

Mixed-signal designs are widely used for applications in segments including automotive, Internet of Things (IoT), communications, industrial control, medical and radio frequency (RF). Verification of these complex mixed-signal ICs is challenging due to the need to ensure they meet demanding specifications with correct connectivity, functionality and adequate system performance across analog/digital (A/D) interfaces on the chip.

To address these challenges, verification teams need to run an increasing number of mixed-signal simulations at the top level as well as at the sub-system level. Their mixed-signal simulation solutions need to be fast, accurate, easy to use, and seamlessly integrate into existing analog and digital verification flows.

Siemens EDA Symphony Mixed-Signal Platform powered by Siemens Analog FastSPICE circuit simulator delivers the fastest mixed-signal simulation performance in the industry without sacrificing the analog accuracy needed for verification. Symphony is the industry's most configurable mixed-signal solution that integrates with all the leading digital simulators to allow maximum re-use of verification infrastructure and offers advance debugging capabilities to improve overall mixed-signal verification productivity. Symphony is tightly integrated with Tanner™ schematic editor S-Edit for analog on top (AoT) designs. With a simple intuitive interface in S-Edit, the designer can set up, launch the simulation, view the results in EZwave™ software, and back-annotation results to the schematic. For an analog mixed-signal design, Symphony supports Verilog, SPICE, Verilog-AMS, VHDL and SystemVerilog.

S-Edit set up

S-Edit is an easy-to-use design environment for schematic capture and design entry. It supports multiple-views per cell including SPICE, schematic, Verilog, Verilog-A, Verilog-AMS, and VHDL views. The designer can select a specific view of a design block for simulation with a click of the mouse in the schematic. As an example, this enables the designer to quickly swap a block for simulation among schematic view, SPICE view, Verilog-A view, Verilog view, etc. With

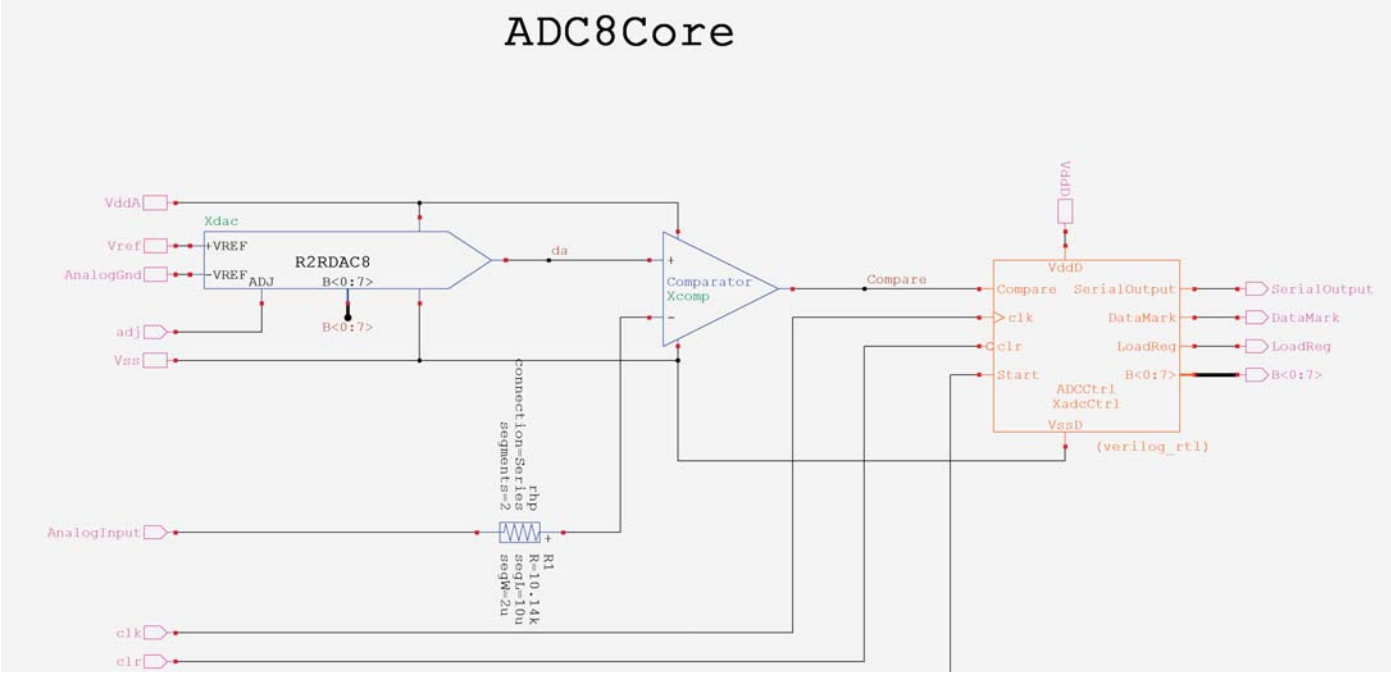

Figure 1: 8 bit ADC design

this swapping, designs can quickly run fast simulation with an abstract model for top-level design to get an overall view of the design, or they can run detailed transistor-level simulation to get final tape-out results.

The following ADC8 design example is an AoT design. The ADCCtrl block has several views, including a Verilog view. All the other blocks are in schematic views. The ADC8 is a simple successive approximation ADC with a R2R DAC, comparator and a control block to do the binary search to match the voltage being converted.

Hierarchy priority

The designer can quickly change the implementation of an instance in the schematic to switch between different levels of abstraction for the block. In this example, we want to use the Verilog implementation of the ADC control block and this is done by performing a right click on the ADCCtrl block in the schematic and choosing the Verilog view to be used when running a mixed-signal simulation. Note S-Edit allows the designer to choose the proper scope for that view. So for the same cell, the designer can choose different implementation views for different instances throughout the hierarchy.

In S-Edit simulation set up dialog, it shows the ADCCtrl block is set to Verilog view for simulation. Note it also pointed out that S-Edit has a default priority. If a block's hierarchy priority is not set, it will follow the default priority order (from highest): Schematic, SPICE, Verilog-A, Verilog-AMS, Verilog, VHDL-AMS, and VHDL. A SPICE view is a text view that has SPICE netlist of the

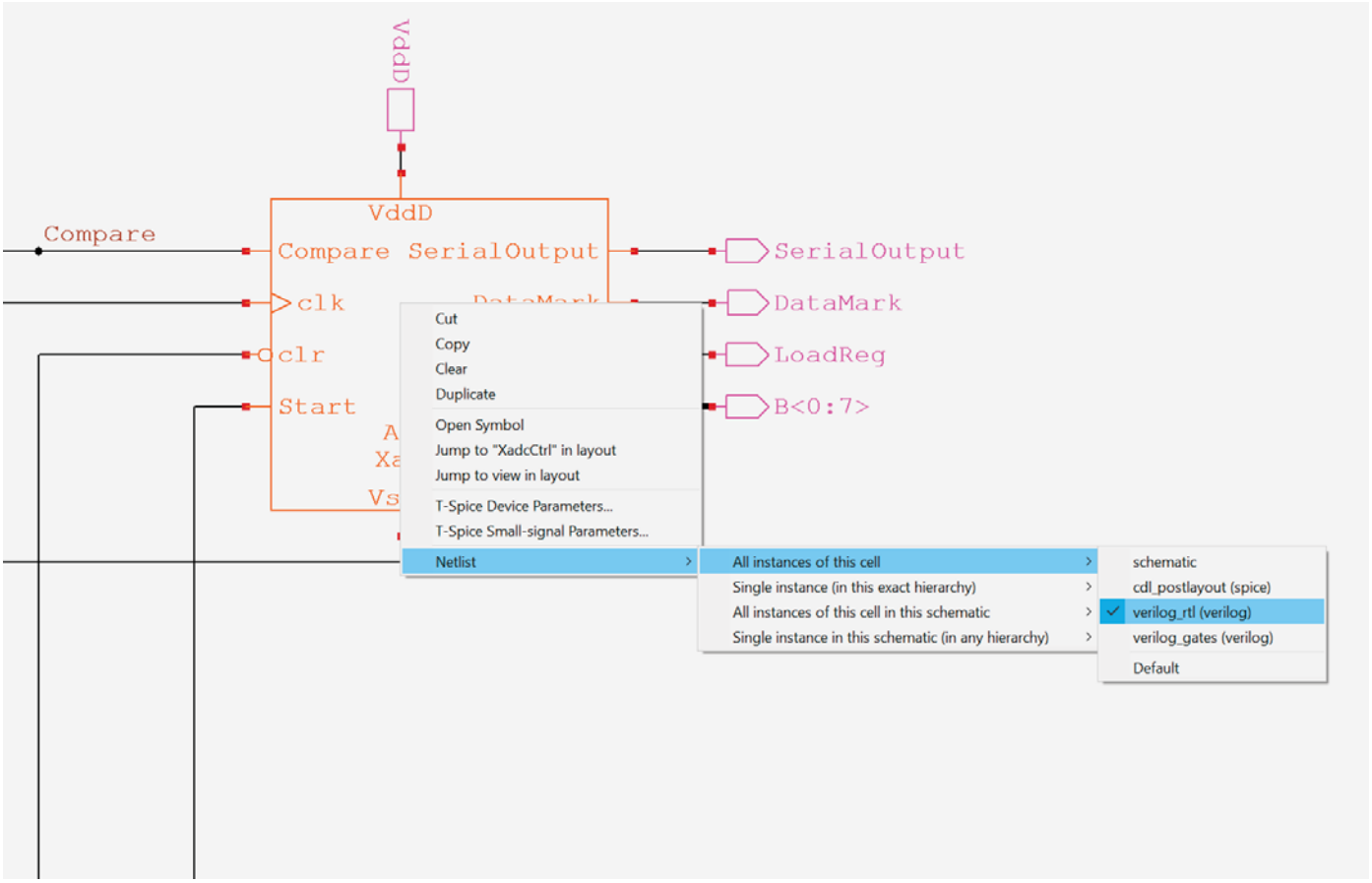

Figure 2: Switch ADCCtrl block to RTL

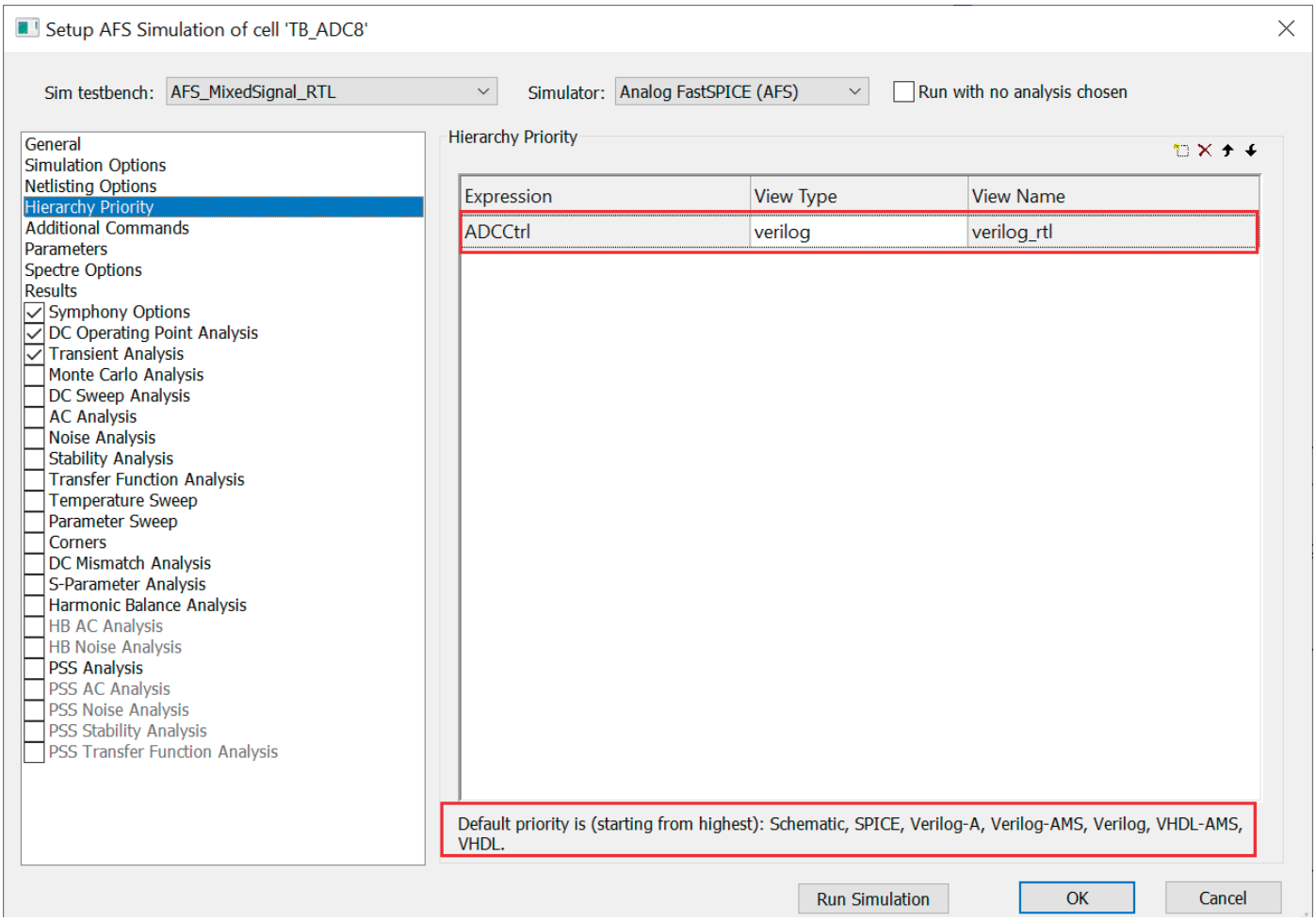

Figure 3: Hierarchy Priority page in Simulation Setup dialog indicates the blocks views that are used for simulation

block and is mainly used for parasitic extracted views to use for post-layout simulation.

Boundary elements

For mixed-signal simulation, the designer will need to tell the simulator how to connect analog and digital signals when crossing a domain boundary. This is done via connect modules, which get automatically inserted at the analog and digital boundaries. These modules are usually created with Verilog AMS code. It is tedious and error-prone. Symphony takes a different approach. It uses boundary elements (BEs), which serve the same purpose as connect modules but are more powerful and easier to use.

Boundary elements are used to connect different domains. Inside a sub-circuit/module, the connections are generally between the same types of ports/nets. However, when sub-circuits/modules in different domains are connected, various combinations of connections may result. These different connection combinations result in the boundary element types, such as Logic (digital) to Electrical (analog) and Electrical to Logic, etc. When a signal crosses a domain boundary (such as analog to digital or digital to analog), Symphony automatically adds in the boundary elements.

In S-Edit, the designer can easily set BEs for different scopes using the GUI. In the Symphony Options pane of the Setup Simulation dialog, the designer can invoke the Setup Boundary Element dialog by clicking the button in the field.

In Setup Boundary Element dialog, the designer can pick the desired scope of the boundary element such as global or only inside a cell or only for specific instances. In the bottom pane, it shows the default values of different parameters of the boundary element. The designer can override them with desired values. When

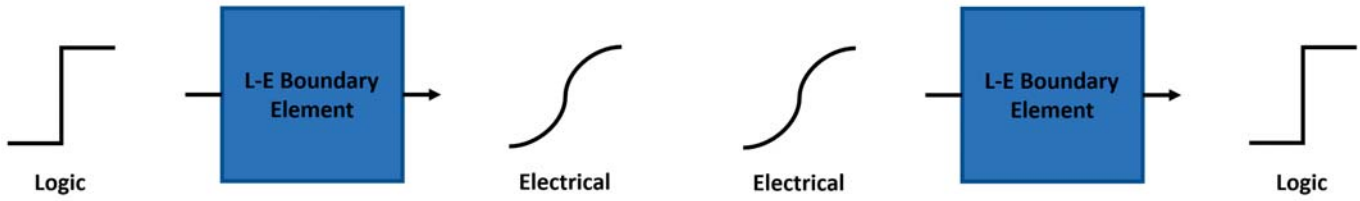

Figure 4: Boundry elements - Logic to Electiral and Electrical to Logic

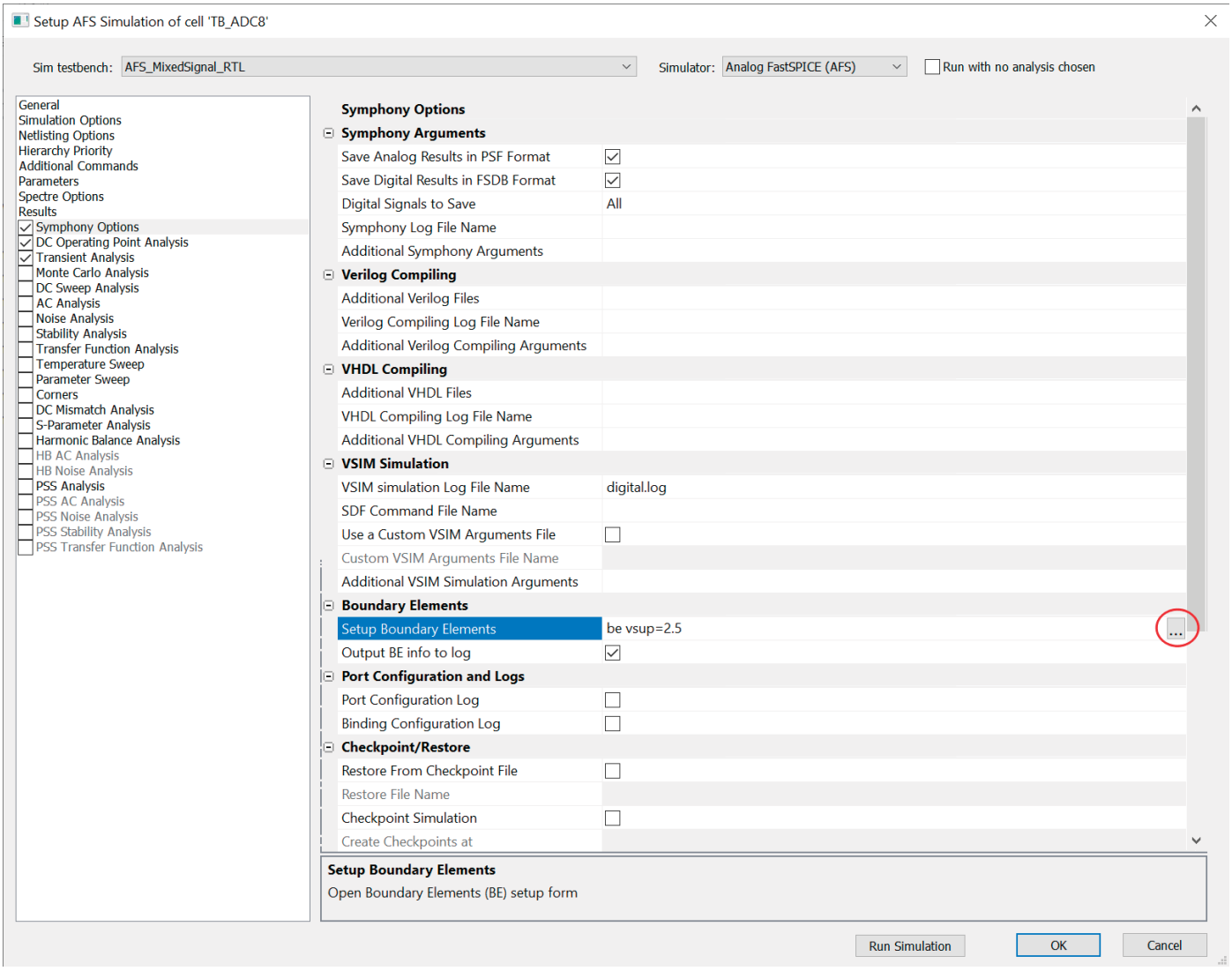

Figure 5: Symphony Options dialog

setting parameters for the specific nets, instance, etc., the designer can use the probe icon to directly pick the net or instance from schematic and its name will be automatically filled in the Scope Applied to column. The minimum information needs for boundary elements is the supply voltage for that domain. Since the example is using logic gates that are designed for 2.5v for high,

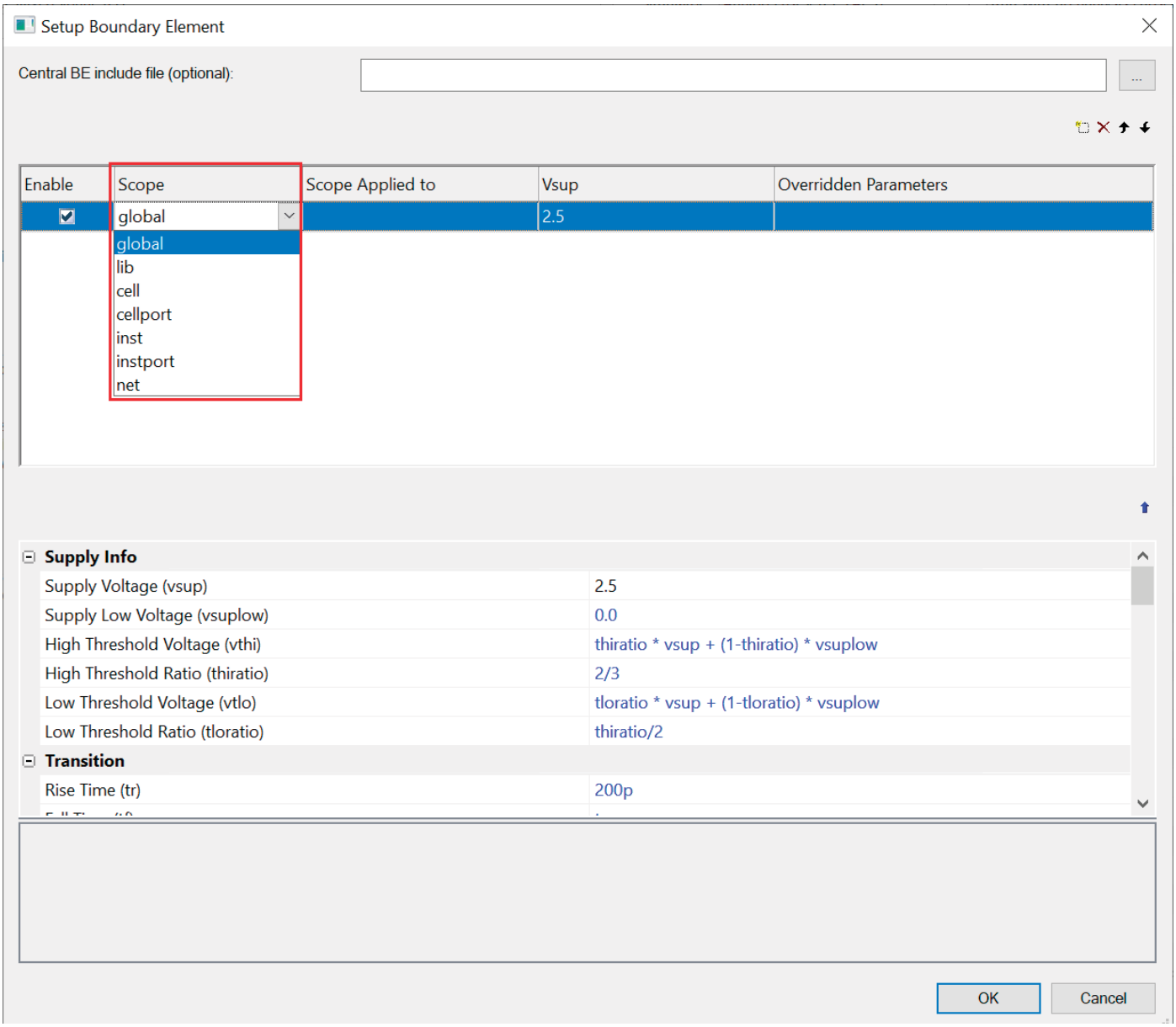

Figure 6: Setup Boundary Element dialog

Vsup was set to 2.5. The supply voltage can also be dynamic based on a voltage in the circuit but this can slow down the simulation.

Simulation logs

In S-Edit command line windows, it logs every editing step the designer does with a TCL command. The designer can quickly modify the command and re-run it to meet their requirements. The designer can also group some commands together into a TCL file and run it to accomplish specific functions.

During simulation, the command line window logs the simulation progress. For long transient simulation, the designer can also hover the mouse over the progress bar at the bottom as shown in the image. It gives

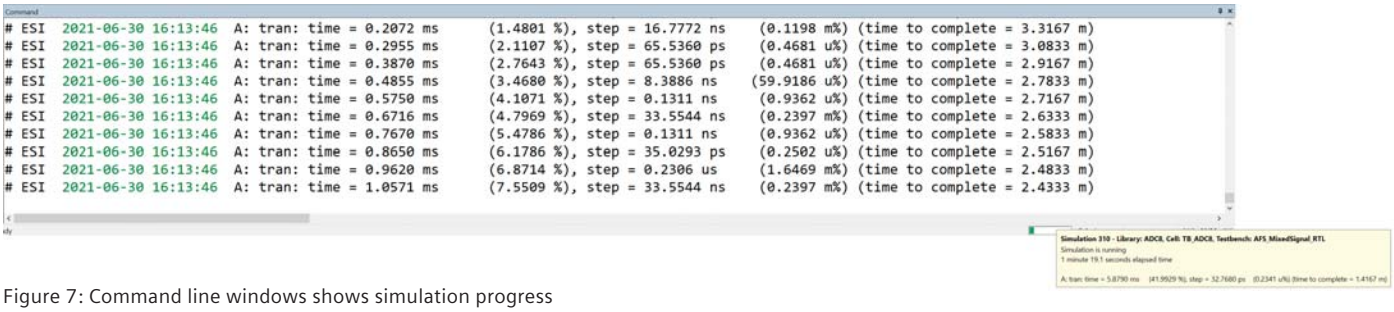

Figure 7: Command line windows shows simulation progress

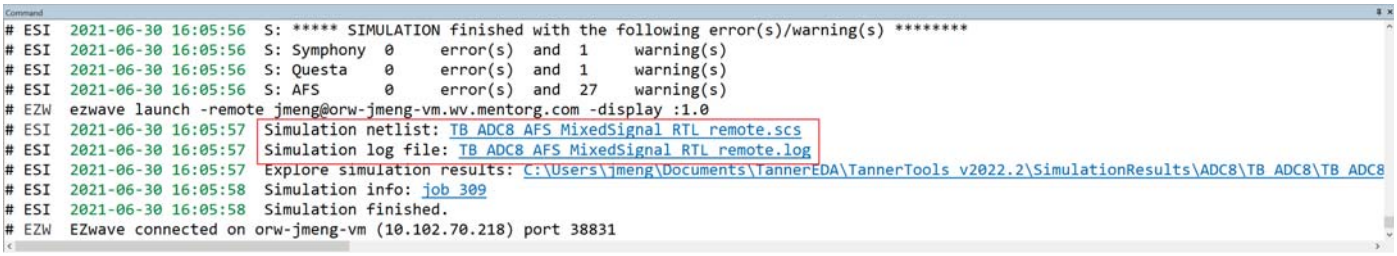

Figure 8: Click hot links in command line windows to quickly open these files

the designer more details about current simulation status.

After the simulation is finished, the command line window shows the hotlinks of the simulation netlist and log file. The designer can open these files with a single click on the link. The files can be opened inside S-Edit, or a in a designated external text editor.

View results in EZwave

In the S-Edit simulation setup dialog, the designer can easily set up which signals to plot after simulation. Additionally, the designer can use expression to generate new waveform or measure data, as shown in the image below. These settings are saved in the design.

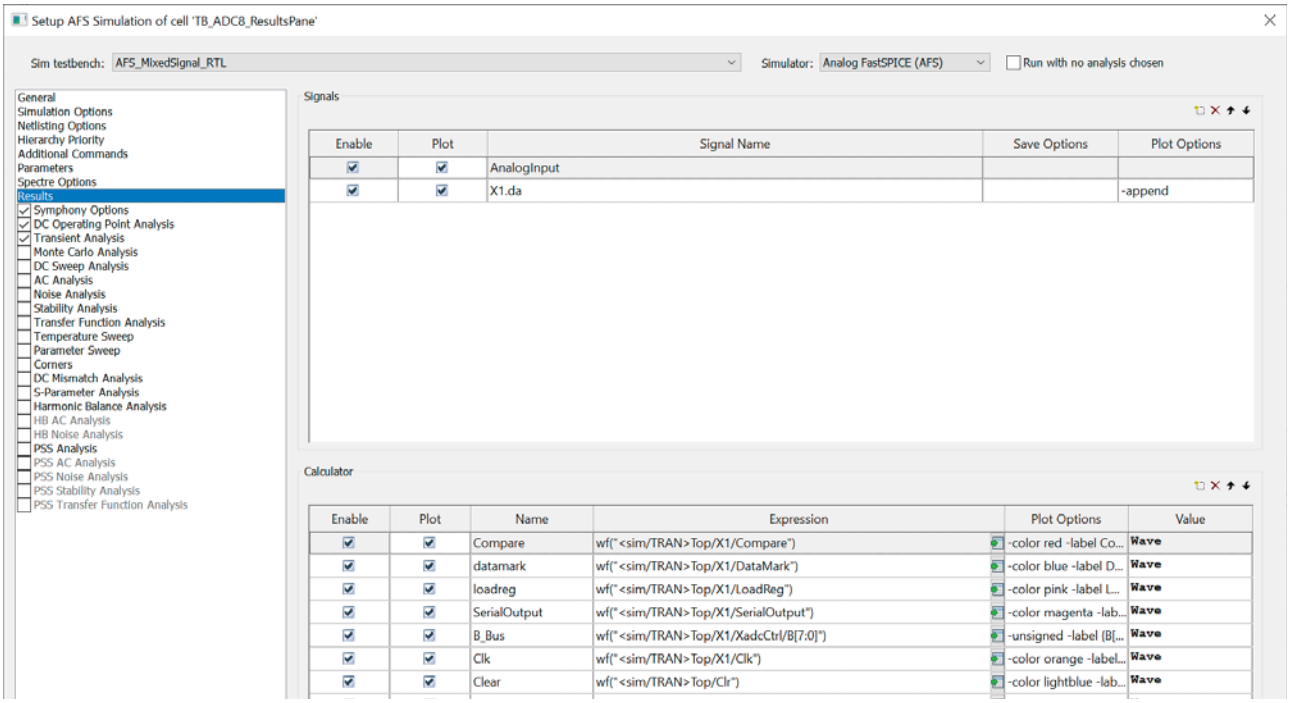

Figure 9: Results pane in Setup Simulation dialog

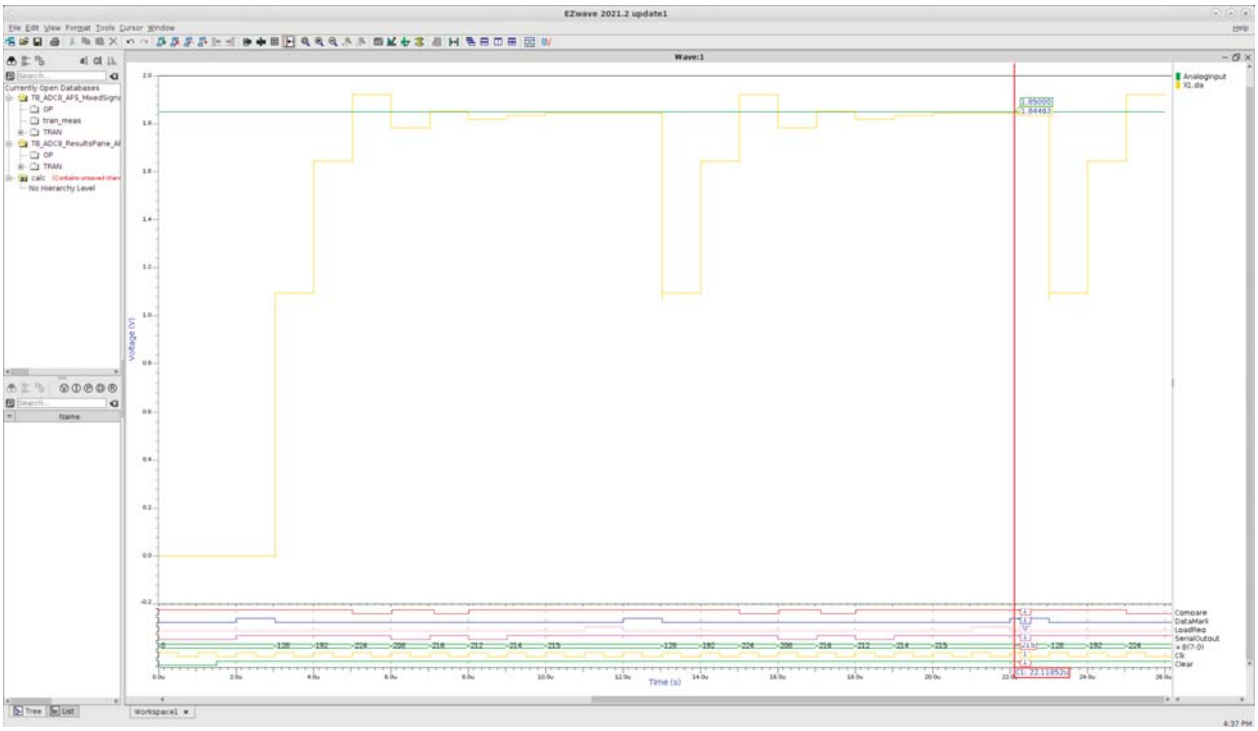

Figure 10: Waveforms in EZWave

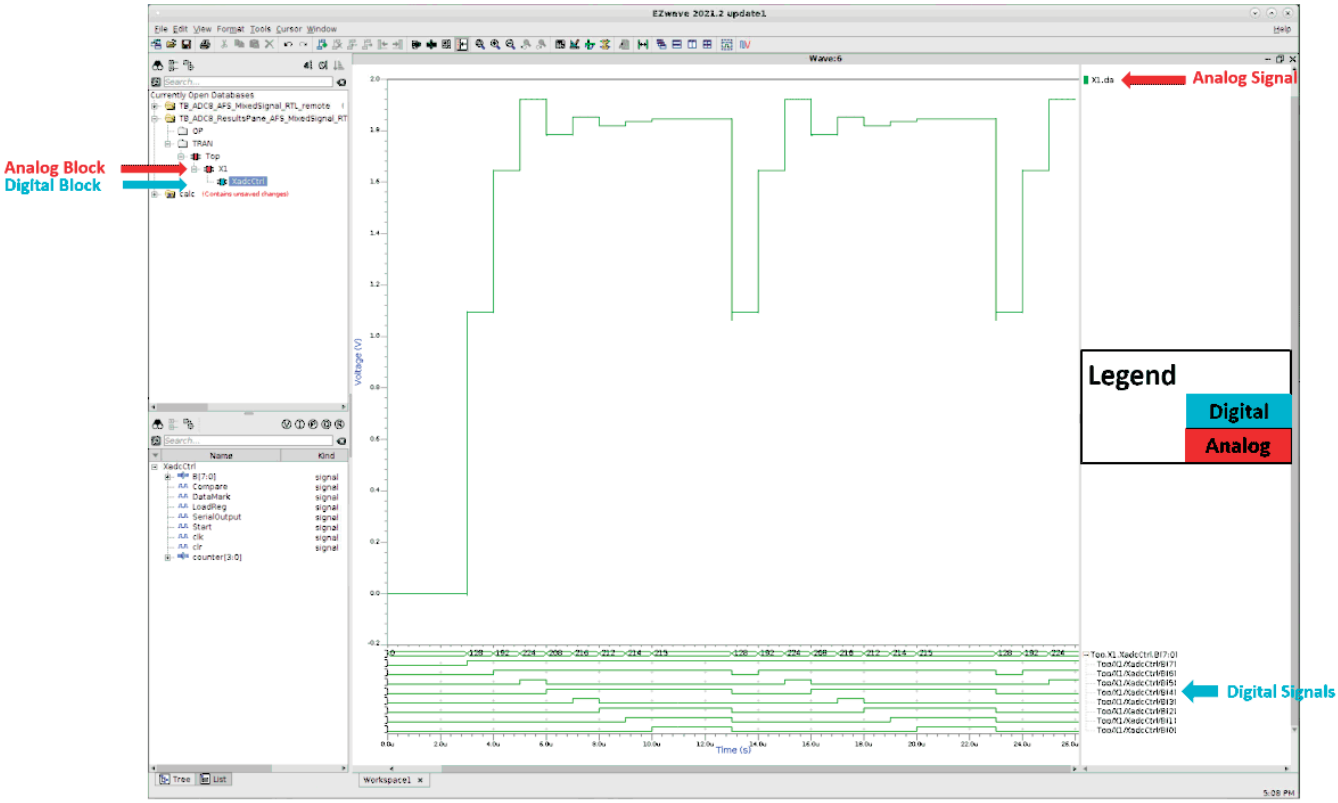

Figure 11: Analog and digital signals in EZWave

The Replot and Recalculate buttons allow the designer to modify the expression or add a new expression without re-running the simulation.

From S-Edit, the designer can probe the schematic and bring up the voltage or current waveform in EZwave, the waveform viewer. The designer can also back annotate operating point value to schematic.

In EZwave the analog and digital signals are displayed side-by-side. The analog and digital blocks are marked with different colors (red for analog and cyan for digital). The analog and digital waveforms are also differentiated with different icons (sine waveform for analog and square waveform for digital). Both the analog and digital signal can be plotted in the same window so they can be analyzed and measured together. The designer can also display the boundary elements in EZwave for further debugging purposes.

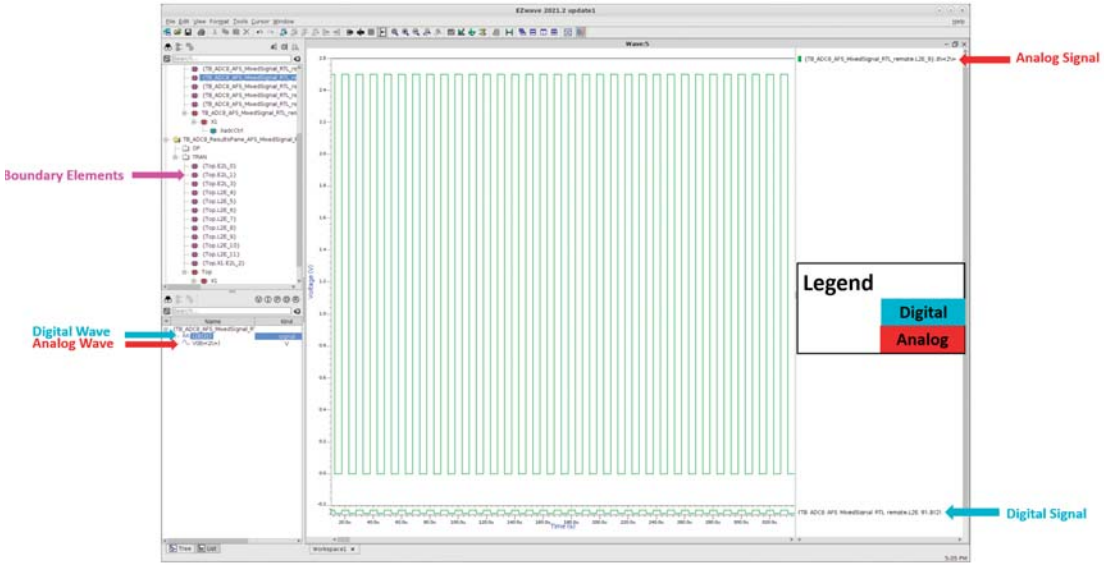

Figure 12: Display boundary elements in EZWave

Conclusion

Analog/Mixed-Signal design and simulation in a Tanner flow is a multi-step process. First, both the analog and digital portions of the design is captured. Next, the simulation is set up, and launched. Finally, when the simulation run or runs have completed the results can be analyzed. With this flow, the user can verify design functionality, connectivity and performance at all levels of the design hierarchy and for all integrated circuit (IC) applications.

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