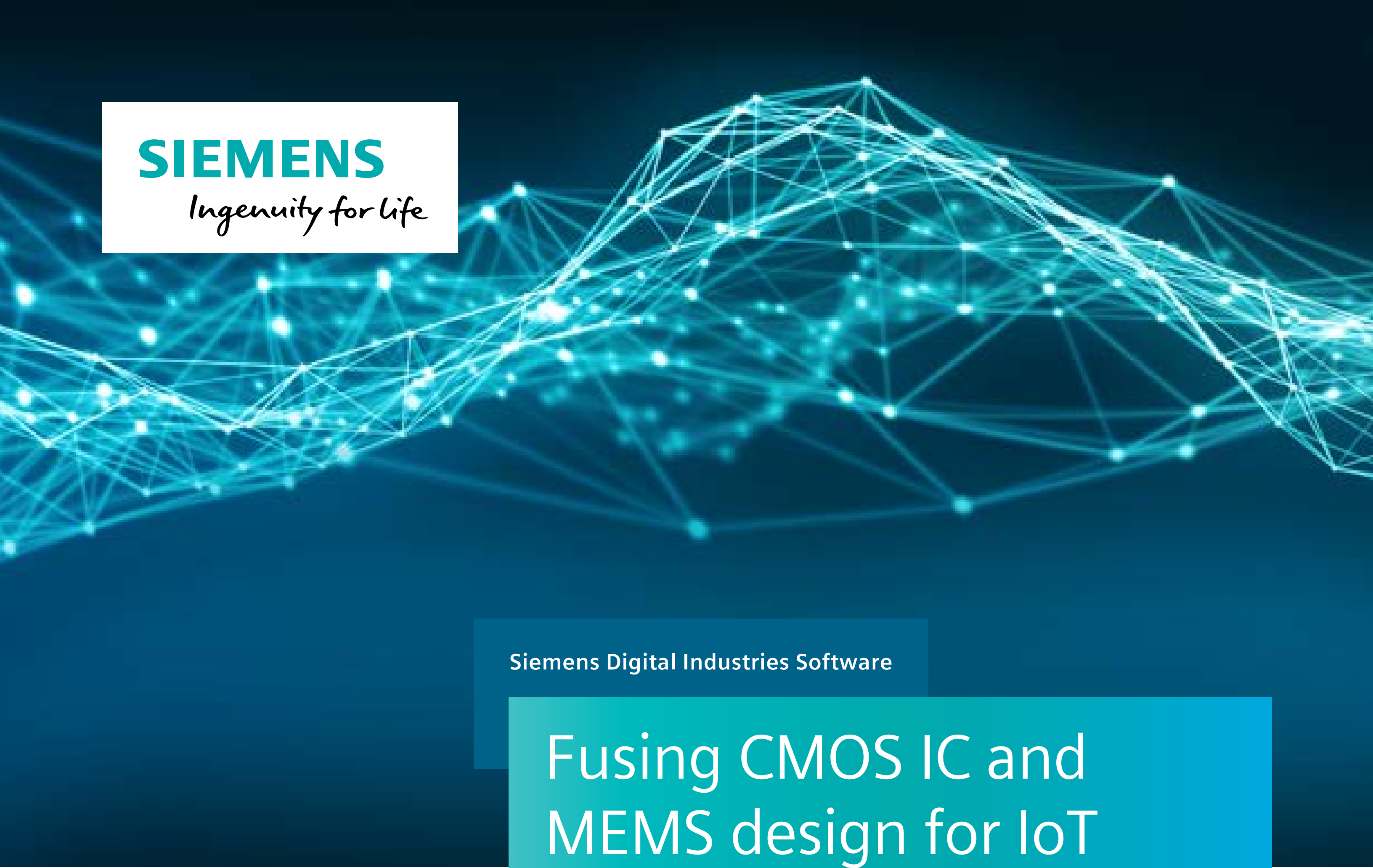

Siemens Digital Industries Software

Fusing CMOS IC and MEMS design for IoT edge devices

Custom IC & MEMS design

Executive summary

Creating a sensor-based IoT edge device is challenging, due to the multiple design domains involved (Analog, digital, RF, and MEMS). But, creating an edge device that combines the electronics using the traditional CMOS IC flow and a MEMS sensor on the same silicon die can seem impossible. In fact, many IoT edge devices combine multiple dies in a single package, separating electronics from the MEMS design. The Tanner AMS IC design flow accommodates single or multiple die techniques for successful IoT edge device design and verification. This paper focuses on the unique challenge of fusing CMOS IC and MEMS design on a single die.

Introduction

Creating a sensor-based IoT edge device is challenging, due to the multiple design domains involved (Figure 1). But, creating an edge device that combines the electronics using the traditional CMOS IC flow and a MEMS sensor on the same silicon die can seem impossible. In fact, many IoT edge devices combine multiple dies in a single package, separating electronics from the MEMS design. The Tanner AMS IC design flow accommodates single or multiple die techniques for successful IoT edge device design and verification. But, this paper focuses on the unique challenge of fusing CMOS IC and MEMS design on a single die.

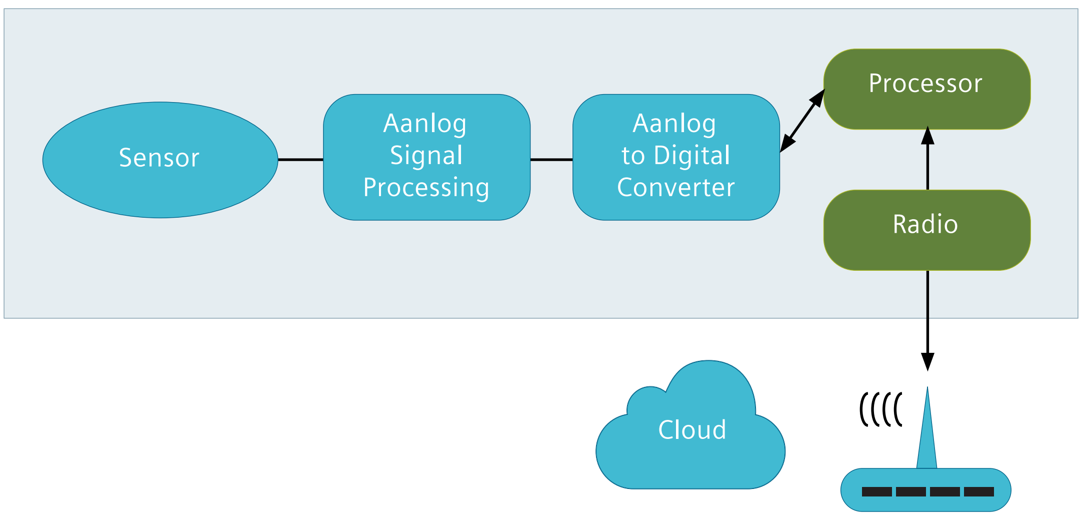

Figure 1: A typical IoT edge device that includes digital, analog, RF, and MEMS domains.

Understanding the design flow

The Tanner design flow (Figure 2) provides a complete environment for AMS IC design.

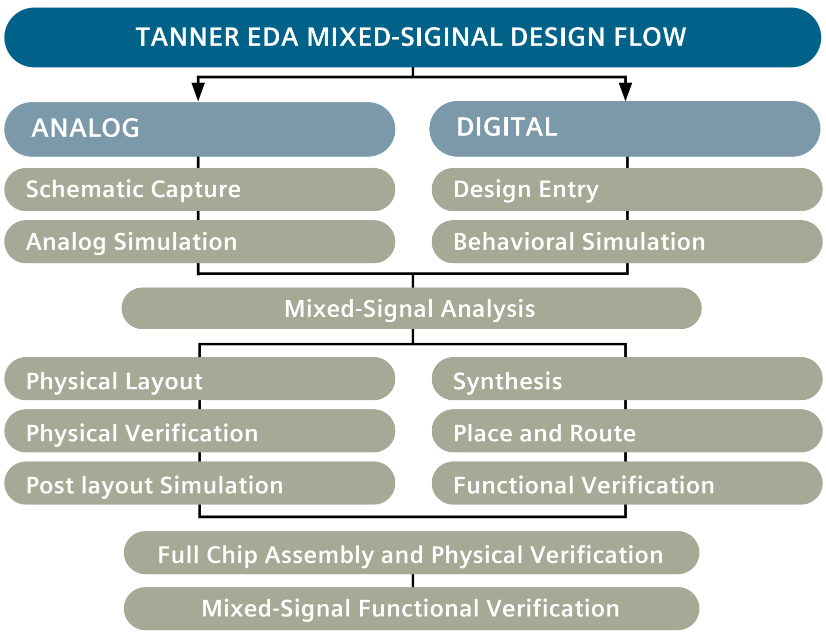

Figure 2: The Tanner AMS design flow.

However, for many years, Tanner has provided customers the ability to interweave MEMS design into this flow, supporting a top-down MEMS IC flow (Figure 3).

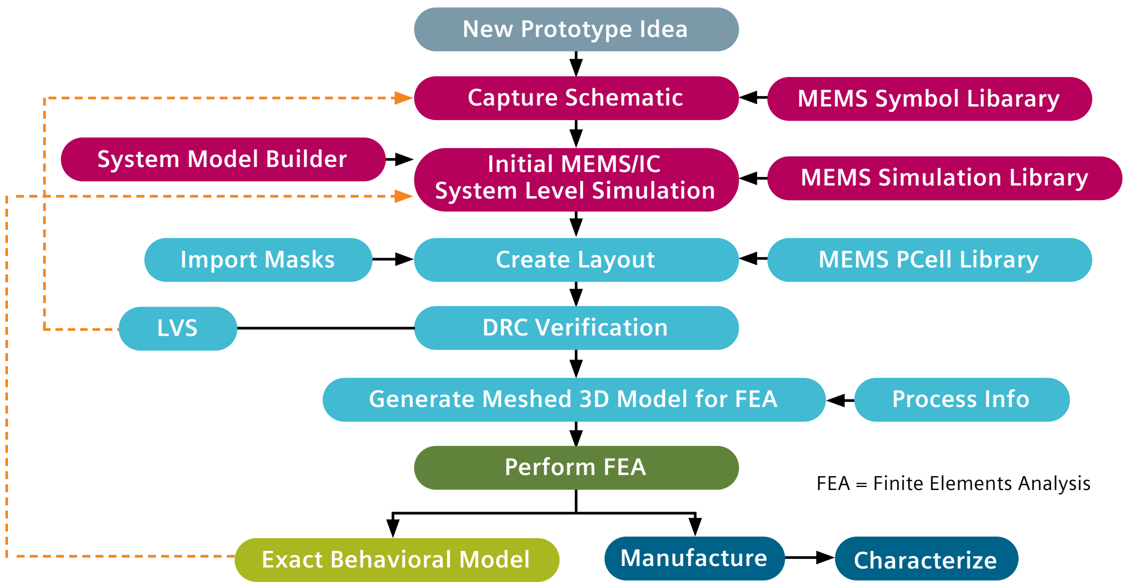

Figure 3: The top-down IC/MEMS flow.

IoT edge design requires that analog, digital, RF, and MEMS design domains are designed and work together, especially if they are going on the same die. Even if the components are targeting separate dies that will be bonded together, they still need to work together during the layout and verification process. The design team needs to capture a mixed analog and digital, RF, and MEMS design, layout the chip, and perform both component and top-level simulation.

Designing the electronics and MEMS on a single die include these interesting points (from Figure 3):

- Schematics can contain IC and MEMS devices. IC devices are modeled using SPICE models and MEMS devices employ behavioral models that are directly modeled in the physical domains such as mechanical, electrostatic, fluidic, and magnetic (Figure 4). MEMS capture is supported by the MEMS Symbol Library within S-Edit.

- In order to support the initial MEMS/IC simulation, you can use the System Model Builder to create a MEMS model using analytical equations in SPICE or Verilog-A. Combined with the MEMS Simulation Library, this allows you to verify that the complete design initially works as expected.
- Using the MEMS PCell library, you can layout the design in L-Edit. In addition, the Library Palette (Figure 5) provides you with basic layout generators for many MEMS devices that you can use as a starting point.

  You can then generate a 3D geometrical model for viewing, virtual prototyping, and to export to finite element analysis (FEA) tools.
- Using the Compact Model Builder, which employs reduced-order modelling techniques, you can create behavioral models from the FEA results for use in final system-level simulation.

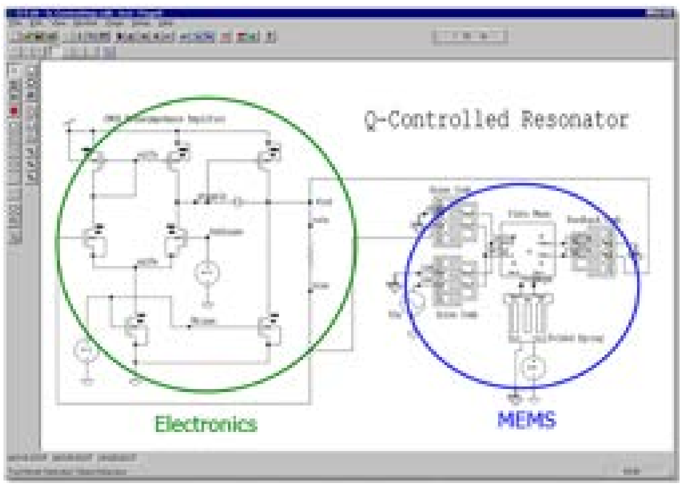

Figure 4: Electronics and MEMS on the same schematic.

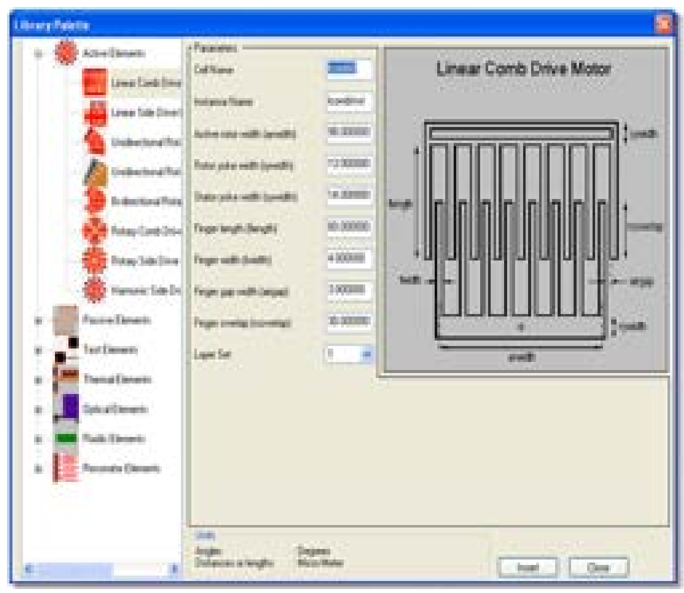

Figure 5: The Library Palette for creating MEMS device Layouts.

Traditionally, the MEMS portion of the design starts by creating a 3D model of a MEMS device and then analyzing the physical characteristics in a third-party finite element analysis (FEA) tool, such as Open Engineering's OOFELIE::Multiphysics, until satisfied with the results. But, you need a 2D mask in order to fabricate the MEMS device. How do you derive the 2D mask from the 3D model? You

Start with 2D mask layout in L-Edit to create the device. The 3D Solid Modeler then takes the layout and a set of 3D fabrication process steps to automatically generate a 3D solid model of your device. Export that 3D model and perform 3D analysis using your favorite finite element tool and then iterate if you find any issues. Make the appropriate changes to the 2D mask layout and then repeat the flow. Using this mask-forward design flow, you can converge on a working fabricated MEMS device because you are directly creating masks that will eventually be used for fabrication, rather than trying to work backwards from the 3D model.

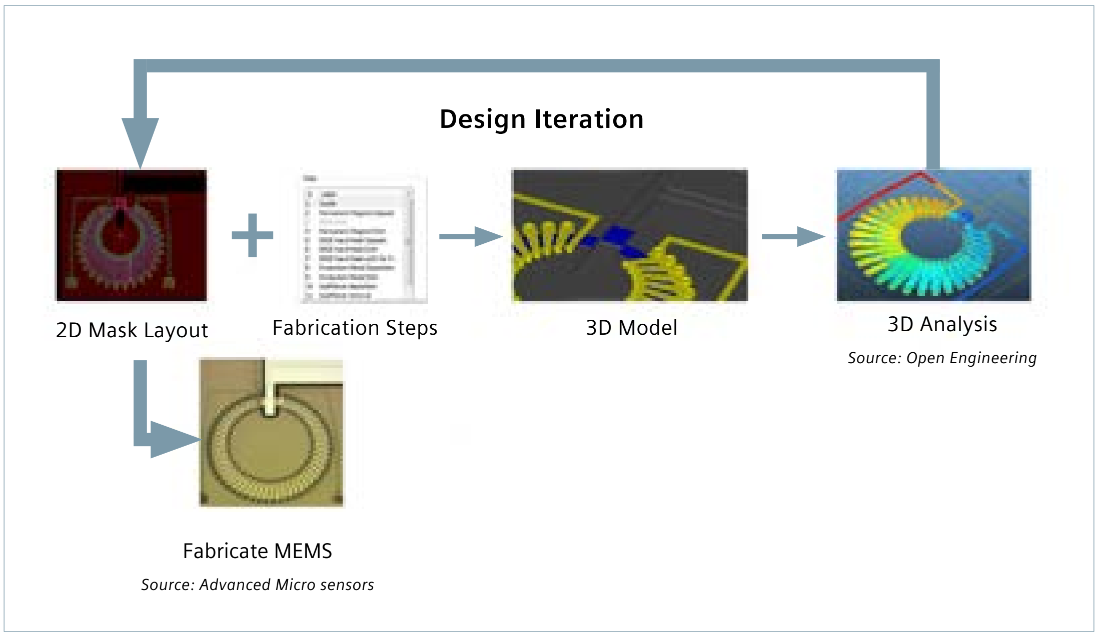

Figure 6: The mask-forward MEMS design flow.

Performing MEMS solid modeling

You can set up the fabrication steps based on foundry process information (Figure 7). Using this information, L-Edit builds up the 3D solid model of your MEMS device for each step of the fabrication process.

You can interact with the resultant 3D model (Figure 8 shows an example) by rotating it, taking cross-sectional views, and you can diagnose fabrication issues. You can automatically export cross-sections for each step of the process to better understand the fabrication process and your device. You can then export the model to an FEA tool for analysis. For more information about preparing for FEA, see the whitepaper here.

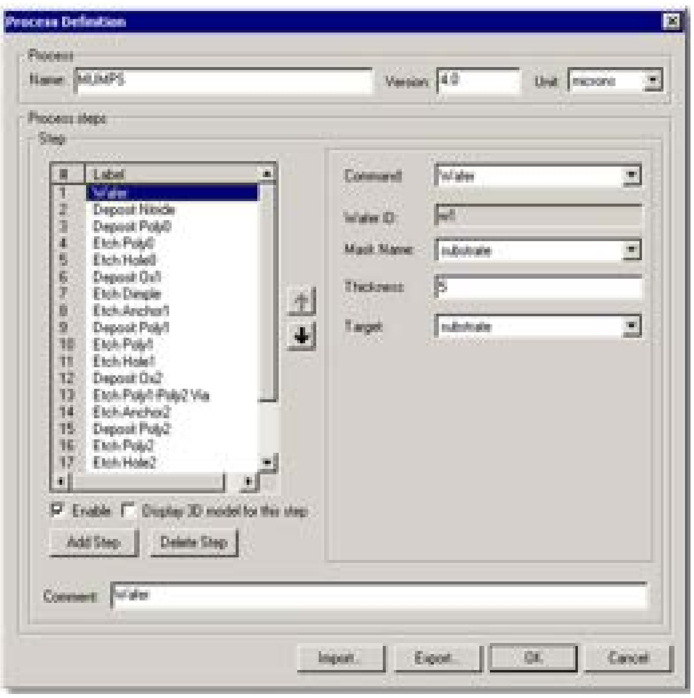

Figure 7: The Fabrication Process Editor.

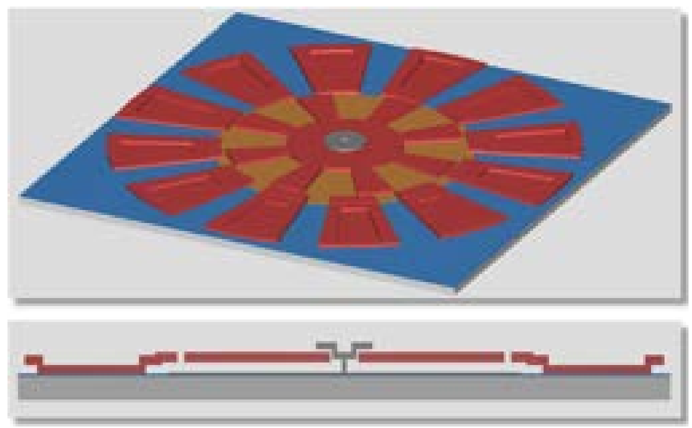

Figure 8: Sample 3D model.

MEMSIC finds success

MEMSIC® Inc. developed a MEMS and CMOS IC accelerometer with no moving parts. Using a unique thermal technology, acceleration is measured by using heated gas molecules (Figure 9). The chips appear in products that require the control or measurement of motion, such as car alarms, mobile electronics, global positioning systems, elevator controls, patient monitoring devices, and head-mounted displays for gaming.

In the center of the 1mm-square sensor is a heater operating at 100°C above ambient temperature. Around the heater are symmetrically placed thermopiles for reporting temperature in different locations. A thermopile is a series of thermocouples, or temperature-sensing elements, connected in a series to boost voltage. The entire sensor is hermetically sealed in an air/gas cavity, outside of which is analog circuitry for amplification, control, analog-to-digital conversion and, in the 3-axis models, digital compensation/calibration circuitry.

In the absence of motion, the thermal profile is balanced among the thermopiles. But any motion or acceleration modifies the convection pattern around the heater, such that the thermopiles in the direction of the acceleration become hotter than the others. The analog circuitry interprets the resulting signal changes from the thermopiles as motion and acceleration.

"Tanner tools have been 100% reliable for us ever since we started using them in 1999. We can work in Tanner tools on MEMS design one minute and analog design the next minute. Plus, we've never had a tapeout error due to verification."

- Yongyao Cai

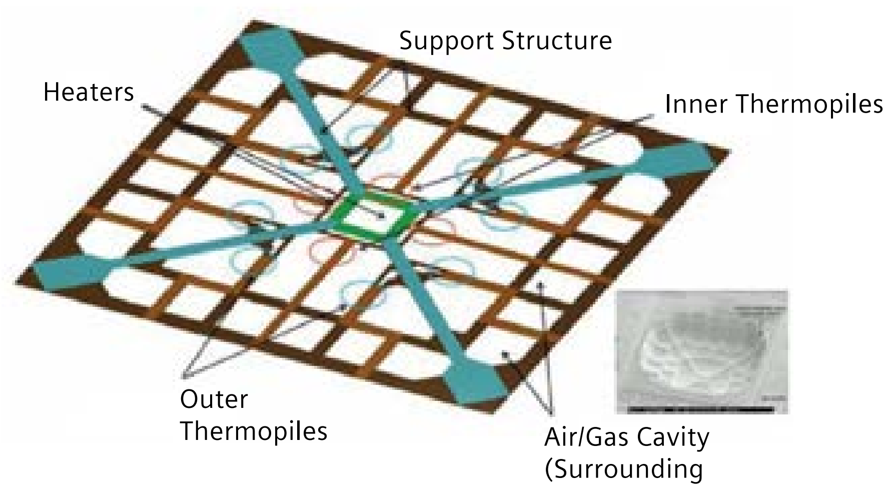

Figure 9: Basic MEMSIC accelerometer structure.

To take advantage of lower fabrication costs, MEMSIC designs its sensors almost exclusively with standard CMOS layers. For example, the heater is gate polysilicon and the first layer of the thermopile is metal and polysilicon.

For the design of accelerometers, MEMSIC engineers use the Tanner flow to create a 3D model directly from the layout for finite element analysis. They use L-Edit to modify the details of the sensor and for layout (Figure 10). After layout, they use L-Edit LVS and L-Edit Standard DRC. Finally, they export from L-Edit to a GDS layout file and send the tapeout to TSMC® for fabrication.

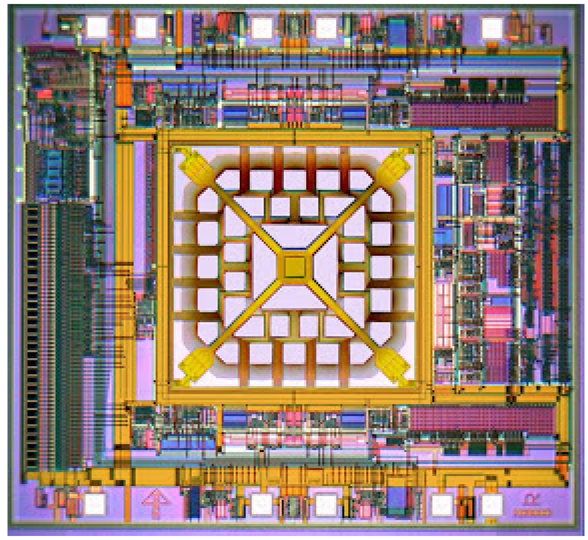

Figure 10: Accelerometer layout using L-Edit.

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