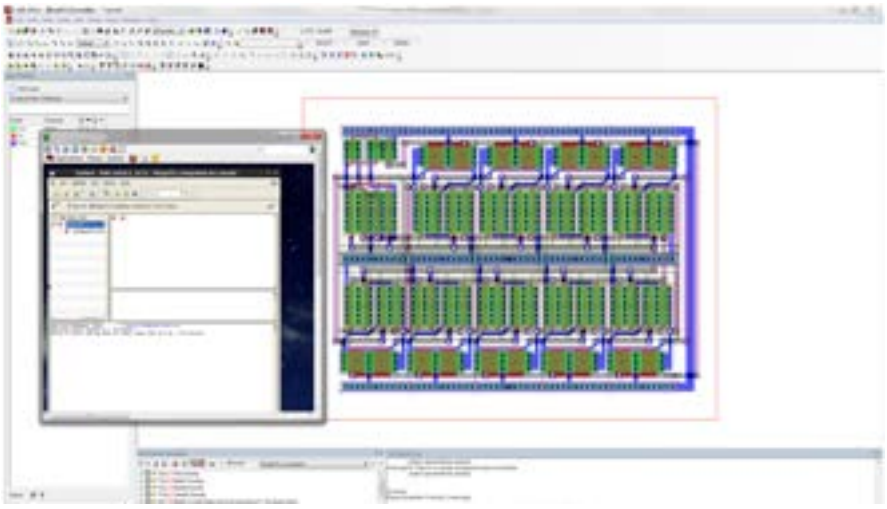
Tanner Calibre One

DATASHEET



Tanner Calibre© One makes it quick and easy to run DRC, LVS, and extraction with Calibre physical verification tools.

The Tanner Calibre One Flow

When performing physical verification of your analog/mixed-signal (AMS) IC designs, speed is the name of the game. Designers need tools that accelerate time to market. These tools must also deliver a level of accuracy that ensures correct-by-design and error-free layouts that must be compatible with the foundry, eliminating the need for time-consuming conversion or modification of command files.

Calibre's physical verification capabilities are the industry standard for accuracy, reliability, and performance. Calibre nmDRC and Calibre nmLVS are the market share leaders in physical verification. Calibre also leads the market with innovative features such as incremental DRC, which ensures designers can complete design rule checking quickly and efficiently. The tools support equation-based design rules, which let designers define continuous, three-dimensional functions that accurately and precisely reflect the complex physical interactions of today's nanometer designs.

Calibre nmDRC Right From the Start

Calibre nmDRC provides the sophisticated and proven technology that enables the fastest and most accurate physical verification of the most challenging designs at any node.

Calibre nmDRC delivers the fastest runtimes in the industry, whether using one CPU or dozens, providing designers with the flexibility needed to optimize resource allocation and usage to meet the desired turnaround time.

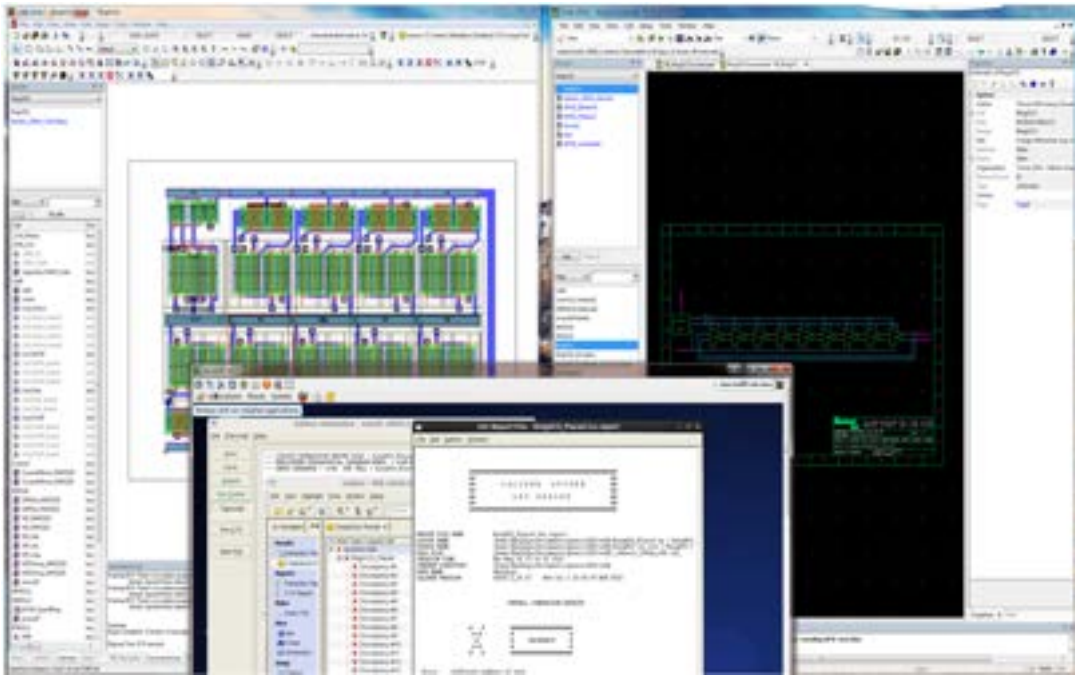
FEATURES AND BENEFITS:

- Tanner Calibre One is a key part of Tanner's complete, full-flow analog/mixed-signal (AMS) IC design suite
- Tanner physical layout editor L-Edit is tightly integrated with Calibre nmDRC, Calibre nmLVS and Calibre xRC
- Intuitive and easy to use - quick learning curve
- Calibre xRC model-based engine calculates intrinsic and coupling capacitances for all nets using the same high degree of accuracy
- Cross-probe between schematic, layout, and LVS report to highlight nets or devices
- Direct access to OpenAccess, LEF/DEF, OASIS, and GDSII design databases
- Calibre nmLVS provides an intuitive and easy to use integrated design verification debugging environment to help find and fix design issues
- Calibre xRC scales across multiple cores or CPUs using the Calibre multithreaded architecture
- Availability of foundry-certified signoff rule decks in SVRF format ensures Calibre xRC parasitic extraction can meet design needs regardless of process or foundry choice

Calibre nmLVS the Next Generation in Circuit Verification

Calibre nmLVS provides the best in class device recognition and parameter extraction for source netlist comparison, and its robust and easy to use integration lets designers insert Calibre nmLVS into the design flow, allowing them to use Calibre as single platform for cell/block and full-chip verification.

Calibre nmLVS is tightly integrated with both Calibre nmDRC and Calibre xRC. Calibre nmLVS enables accurate circuit Verification because it is able to measure actual device geometries of the full chip for complete accounting of physical parameters.



Calibre xRC Fast, Accurate, Rule-Based Parasitic Extraction

Calibre xRC is fully integrated into the Calibre verification suite for seamless creation of netlists and parasitic debugging in the design environment using Calibre RVE. Calibre xRC performance is derived from the core Calibre hierarchical engine, and is therefore not tied to one particular design style. Calibre xRC delivers unparalleled performance on ASIC, memory, analog, and SoC designs with no trade-off in accuracy.

Calibre RVE Graphical Results Viewing Environment

Calibre RVE™ brings the solution together, providing a graphical results viewing environment that reduces debug time by visually identifying design issues instantly and cross-selecting the associated issue in L-Edit and S-Edit.

The Tanner Calibre One IC verification suite is an intregated solution within the complete analog/mixed-signal design environment offered by Tanner EDA. Confidently tape out your designs with this verification suite.

For the latest product information, call us or visit: www.mentor.com/tannereda

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