DIGITAL INDUSTRIES SOFTWARE

Using AI for advances in test

Technology brief

Executive summary
This document summarizes the usage of AI in Tessent products from expert user automation to machine learning. We summarize capabilities available to you today and ongoing work on potential improvements embedding AI in our automation.

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Tessent perspective on automation

The goal of electronic design automation (EDA) is to simplify the design tasks and enable greater capabilities using automation embedded within software tools.

Siemens EDA tools embed three types of AI within them as shown in Figure 1. Analytical AI solves problems algorithmically and creates more intuitive tools and processes. Predictive AI uses training and previous learnings to predict and improve results. Generative AI creates new insights and methods with self-learning.

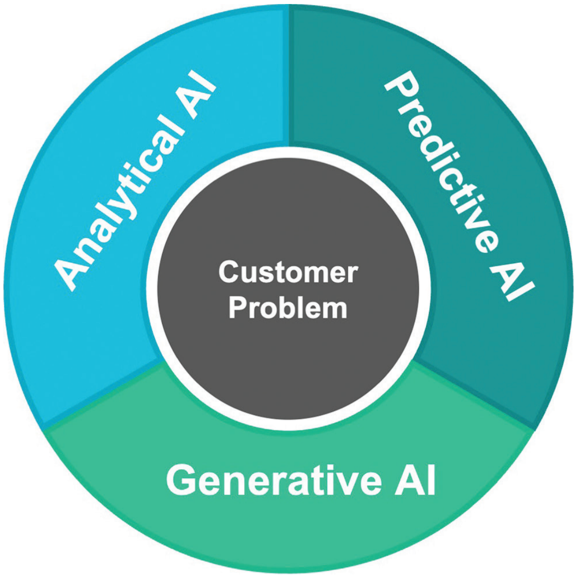


Figure 1. AI solutions built with verifiability at their core.

> “Tessent’s charter is to provide highly automated solutions proven and tuned on real silicon prior to release.”

When using EDA tools, you want to be confident that the tools are effective and robust. This is a basic principle within Tessent and how we develop products.

At Tessent we have proven AI methods and machine learning technologies deployed. We continue to enhance other areas within our products with AI methods.

Users have better things to do with their time than to play with variables and adjust tool settings. The Tessent approach is to solve problems as much as possible algorithmically, so users don’t need to worry about detailed tradeoffs. If the best result is to proceed with a certain sequence, adjust based on observed data and proceed, then it can be embedded algorithmically. Similarly, if a full interpretation of results requires additional tests and reports then those can be run and set up ahead of time. This is the type of automation is commonly embedded within the Tessent algorithms.

Additionally, a user needs to understand how a tool decision was made and have the ability to perform tradeoffs. Explainability of the results from algorithms has been a cornerstone of our approach. We empower users with both algorithms that optimize and then present the trade-offs that were made. If the user wants to explore other options, for instance prioritize one parameter, then they can adjust the operation sequence to accommodate their workflow.

There are cases where companies want to build their own special type of company-specific customized flows. This is made possible with the Tessent Platform environment. Within the Platform, the user has access to ”introspect” data of which the tool is aware and may build custom scripts for their special needs. This gives the user the ability to create tool-level features, design rule checks and more, and register them as commands.

ATPG Expert

Embed user knowledge and decision-making within the tools

Expert systems are a simple form of AI which mimics the knowledge and decisions of an expert user. A few expert systems were embedded within Tessent Automatic Test Pattern Generation (ATPG) to simplify the ATPG process.

“ATPG Expert” was built to simplify the task of analyzing the design to determine the best parameters to set for an ATPG run. The goal is to optimize coverage and pattern count automatically.

Previously, these types of decisions would have varying results depending on the user’s knowledge. To make work easier, ATPG Expert decides on the most appropriate settings based on design characteristics. This includes:

- Which clocks to pulse
- Abort limits: based on design complexity how many “tries” before aborting on a targeted fault
- Contention checks
- Sequential depth: how many pulses to apply after shifting is complete to load non-scan cells prior to capture
- ... and more

Furthermore, a user can just set the parameters and then start a session creating patterns. The ATPG Expert capability being embedded in the software algorithms can view the results during an ATPG run and adjust mid-run. Therefore, ATPG Expert can adapt during the session and adjust to re-optimized parameters based on the progress it observed.

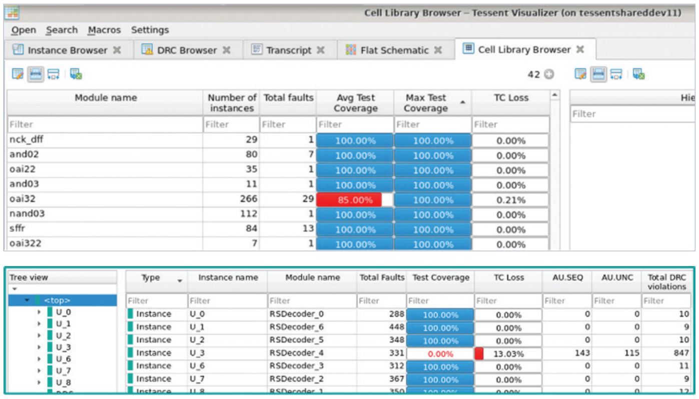
These types of algorithmic adjustments, which are beyond human capability, are referred to by Tessent as “analytical AI.”

Automated debug

A second expert system is sometimes referred to as “fault grouping.” Many times after running ATPG, you might need to run a few experiments to debug missing coverage. Much of the data from these types of experiments are now embedded in the ATPG run. Once the run is complete, there is a summary of various types of fault categories and coverage impact. There is no need for additional tests.

Some of the types of information automatically provided are:

- Grouping of AU faults: AU faults are determined to be ATPG Untestable. These are now further broken down into specific categories such as in IJTAG logic (AU.IJTAG), OCC logic (AU.OCC), and more
- Sequential fault depth: a summary of % of faults not detected because they need a higher sequential nonscan cycle depth
- Constrained pins: a breakdown of total loss of coverage due to each constrained primary input pin
- Constrained cell: a breakdown of internal registers that are learned to initialize to a static state and stay there and how much they impact coverage
- Coverage loss by clock domain: this is also shown in the Tessent Visualizer GUI application to give a simple hierarchical view of coverage loss sorted by capture clocks



Module name	Number of instances	Total faults	Avg Test Coverage	Max Test Coverage	TC Loss
nck_dff	29	1	100.00%	100.00%	0.00%
and02	80	7	100.00%	100.00%	0.00%
oai22	35	1	100.00%	100.00%	0.00%
and03	11	1	100.00%	100.00%	0.00%
oai32	266	29	85.00%	100.00%	0.21%
nand03	112	1	100.00%	100.00%	0.00%
sffr	84	13	100.00%	100.00%	0.00%
oai322	7	1	100.00%	100.00%	0.00%

Type	Instance name	Module name	Total Faults	Test Coverage	TC Loss	AU.SEQ	AU.UNC	Total DRC violations
Instance	U_0	RSDecoder_0	288	100.00%	0.00%	0	0	10
Instance	U_1	RSDecoder_6	448	100.00%	0.00%	0	0	9
Instance	U_2	RSDecoder_5	348	100.00%	0.00%	0	0	10
Instance	U_3	RSDecoder_4	331	0.00%	13.03%	143	115	847
Instance	U_6	RSDecoder_3	312	100.00%	0.00%	0	0	11
Instance	U_7	RSDecoder_2	367	100.00%	0.00%	0	0	9
Instance	U_8	RSDecoder_1	350	[illegible]	[illegible]	0	0	12

Figure 2. Tessent Visualizer can summarize coverage loss due to library models, capture clocks, and as shown hierarchical instances and modules.

Machine learning to find trends in scan fail data

AI can find yield limiters that are hidden from humans.

Semiconductor production yield has a direct impact on a product's profitability. It is vitally important to quickly get the yield high enough for volume production and to find opportunities to improve yield when in volume production. AI's strength is combining more data, building up higher level relationships and uncovering additional yield limiters.

Expertise-based AI was first employed about 15 years ago to improve scan diagnosis. This type of probability-based diagnosis grouped faults based on known/expert characteristics. This filters many candidates into the most likely suspects. This was found to result in more than 5x fewer suspects in a diagnosis call-out.

Semiconductor production can be in the millions and has lots of scan fail data available. The analysis of a large number of scan fail data from volume diagnosis for yield limiters lends itself into machine learning to find trends that are hard for a human to recognize. Tessent employs unsupervised machine-learning (Brady Benware, 2012) but with some limited guidance. The results were a few notable capabilities that improved identification accuracy and resolution of yield limiters. Some examples of this form of machine-learning are:

- **Profiling-based chain diagnosis:** This method was implemented in Tessent tools more than 10 years ago. It improved diagnosis accuracy by 2x and improved resolution by >2x fewer suspects. The same method was applied to logic diagnosis as well
- **Root cause deconvolution (RCD):** First published about 10 years ago. RCD hides the noise from the likely suspects (Brady Benware, 2012). It has been proven in Pareto charts across more than 10 nodes, including down to 3 nm. One recent case study of RCD in production in 2023 but not published at the time of this paper is a production yield improvement of 2.5% in an already high yield product
- **Population-based statistical diagnosis:** Improving beyond RCD to further weed out suspects are not important. An electrical fault isolation (EFI) case published in ISTFA 2021 described avoiding EFI on 2.4x additional failing die, which resulted in more than $1 million dollars of savings a month.

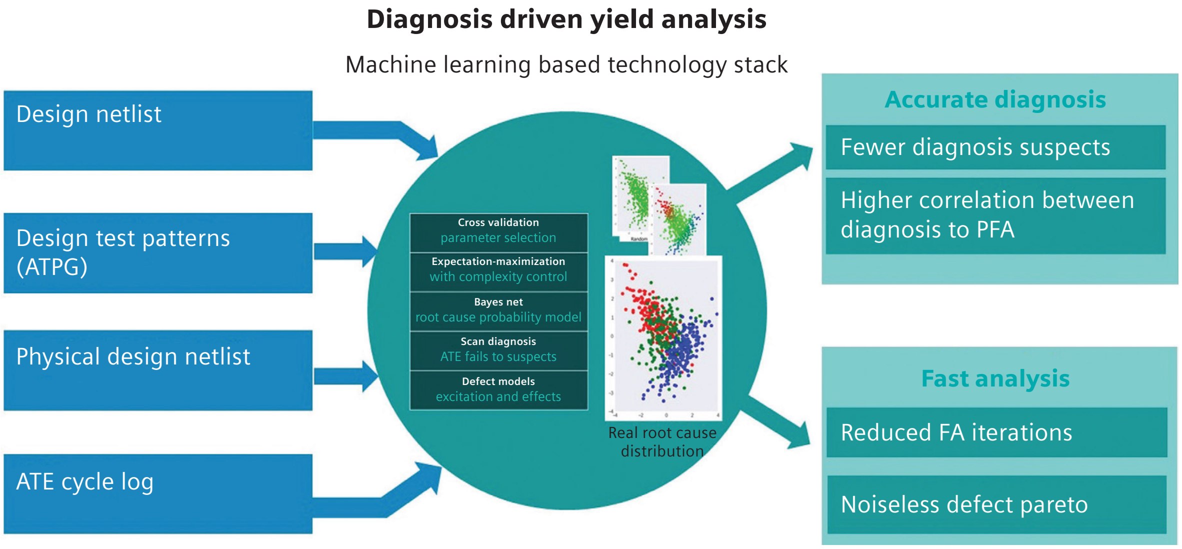


Figure 3. The application of machine learning to improve yield.

DFT planning and tradeoff optimization with many variables

One of the best solutions to a complex problem is to change the problem so that it is simpler.

When designing a full SoC there are many tradeoffs related to the DFT architecture. A top-level DFT architecture traditionally needs to balance and optimize the following parameters:

- Within each core
  - # input scan channels feeding embedded compression
  - # output scan channels from embedded compression
  - Size of the pattern set generated for the core
  - Length of the scan chains in the core
  - Number of scan chains based on available scan channels
- At the top level
  - # of IO pins available to provide scan data
  - Power constraints from running multiple cores in parallel
  - A test access management (TAM) mechanism to test groups of cores. The simplest form is a large mux structure from core output channels to chip IO pins controlled by a test mode setting

It often takes many iterations as the core designs evolve to produce an effective DFT architecture.

Some users state that they required hundreds of iterations when planning their DFT architecture. It is very difficult to select the best set of cores to test in parallel and balance how many of the available IOs to route to each; some cores may have different scan chain lengths. This gets complicated because the pattern size varies between cores which impacts how many scan channels (bandwidth) to apply to each core. As the core designs evolve, their scan channel requirements may change; a pattern set's size may be different than expected necessitating further iterations. Given a design with 100s of cores, you would need to potentially balance 1000 variables, many of which change during the design development.

DFT architecture design has a direct impact on time to market and suffers from design and resource trends.

The DFT architecture challenge is harder with newer, more complex designs. These designs continue to scale in total numbers of cores, gate count and numbers of identical cores. At the same time, often the number of IO pins available for test is reducing and the availability of skilled DFT engineers is reducing. This challenge is summarized in the figure 4 below. If you wait until all the core designs and patterns are complete, then there are many variables that must be balanced and the core DFT designs reworked to balance the bandwidth available from the IO.

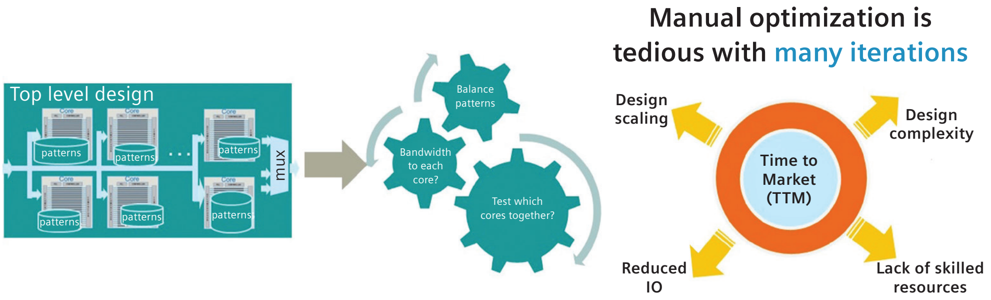


Figure 4. Tradeoffs necessary when designing an SoC complicated by design and resource trends which further impact time to market.

In addition to the trouble balancing all the variables to design test modes and allocation IO pin bandwidth, the traditional solution is usually static. A DFT architecture often doesn't have a lot of flexibility to adjust for issues such as additional patterns found to be necessary, Engineering Change Orders (ECOs), adjustments to cores tested in parallel, or other late changes or observations.

A new DFT architecture

Change the problem so these many variables don't exist

Tessent Streaming Scan Network (SSN) provides a new type of DFT architecture that removes the difficult tradeoffs mentioned above. SSN uses a packetized data delivery mechanism for scan data. Any size SSN bus can be used to deliver data to any size scan channels at various cores. Thus, there is no need to iterate on balancing IO to cores, or even to have a top-level test access mechanism (TAM).

A huge benefit from SSN is that core DFT insertion and pattern generation can be completed when that core is ready. There is no need to wait for other cores and re-balance and adjust the core. This is a dramatic improvement in DFT architecture time to market. All the variables that traditionally needed to be balanced are now not a factor. Some well-known industry leaders have reported as much as 10x productivity improvement when utilizing SSN (Côté, et al., 2020).

When the final design is complete, the user can decide which patterns to apply to which cores in parallel. At that point, SSN algorithms automatically balance the packet data for each core such that the tests of the groups of cores all complete around the same time. This optimization can happen at any time and can be changed at any time. It is another form of "analytical AI" since the tool performs the optimizations and can be adapted at any point.

An additional benefit of SSN and using packetized scan delivery mechanism is that each core operates independently when the packet data is delivered. Clock generation exists at each core's SSN interface to perform clock strobes for shift and capture operations. This means that there is no longer a need to close timing for scan_en or shift clocks throughout the entire design. Timing closure is greatly simplified. Even more significant is the impact on power during test. Cores shift and capture independently so the power during scan test is greatly reduced. This is even true for identical cores since their input data is shared but serially transferred to each identical core. Cores will shift when their packet data is available; it doesn't need to wait or align with any other core.

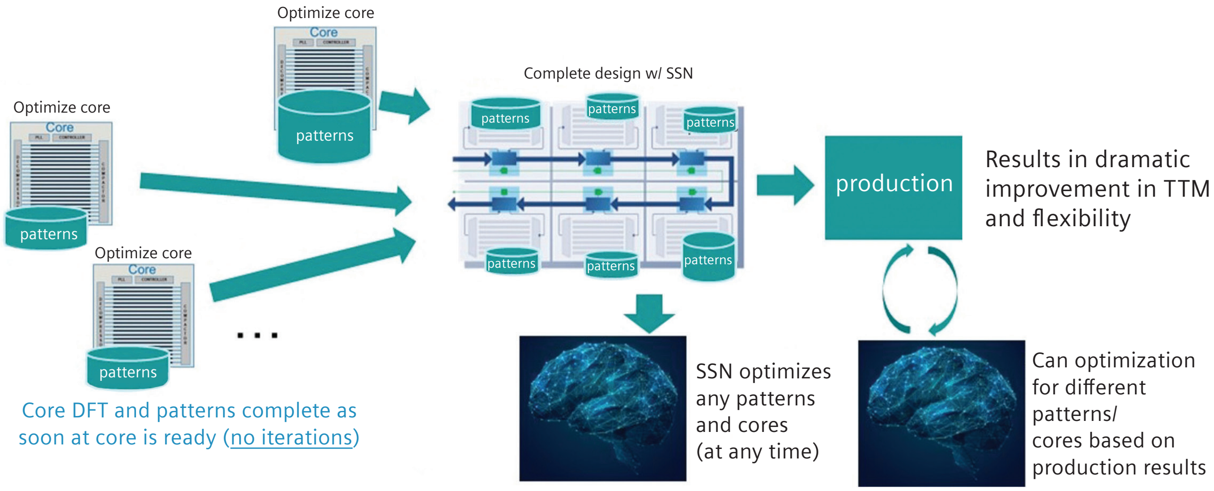

Optimize core
Core
patterns
Optimize core
Core
patterns
Optimize core
Core
patterns
. . .
Core DFT and patterns complete as soon at core is ready (no iterations)
Complete design w/ SSN
patterns
patterns
patterns
patterns
patterns
patterns
production
Results in dramatic improvement in TTM and flexibility
SSN optimizes any patterns and cores (at any time)
Can optimization for different patterns/ cores based on production results

Figure 5. SSN removes the need to trade off and optimize core scan channels/patterns with the embedding and IO pins available.

Looking forward

Training DFT tools to learn and guide users.

Layout pattern systematics
Tessent has partnered with PDF Solutions to find layout patterns that are prone to fail (Cheng, et al., 2017). This big data analysis presents an opportunity to improve yield by an additional 1-3%.

Training ATPG on circuit structures
Machine learning has a potential to perform optimizations on ATPG by learning certain characteristics about a design (Joe, Mukherjee, Pomeranz, & Rajski, 2022). If there is a similar design or the design undergoes an ECO, the tools can take advantage of what specifically has changed compared to what was learned in the baseline. A full ATPG run is not required.

Knowledge access acceleration
There is a broad opportunity to help automate or guide the user to effective results quickly. This is especially important for businesses that have trouble finding resources skilled in DFT. Using a co-pilot flow/methodology guidance can be helpful for new and experienced users. Instead of having to know all the details, the tool could assess where the design is in the DFT insertion or pattern generation process and guide them forward. Many of the lower-level detailed operations can be automated based on higher level intent commands.

Another opportunity is to perform experiments to find the optimal configuration for DFT, compression configuration or ATPG for a particular design. Our customers have already experienced up to a 5x pattern application time improvement using a prototype compression advisor utility.

In summary, test tool technology has tried to simplify and automate design tasks algorithmically. Some features you have access to include automation to adapt during the sessions. In some cases, the size of the data is beyond simple algorithmic solutions such as with yield learning and the usage of machine learning. Going forward, we are aggressively working on AI technologies to provide additional benefits for your DFT and design work.

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