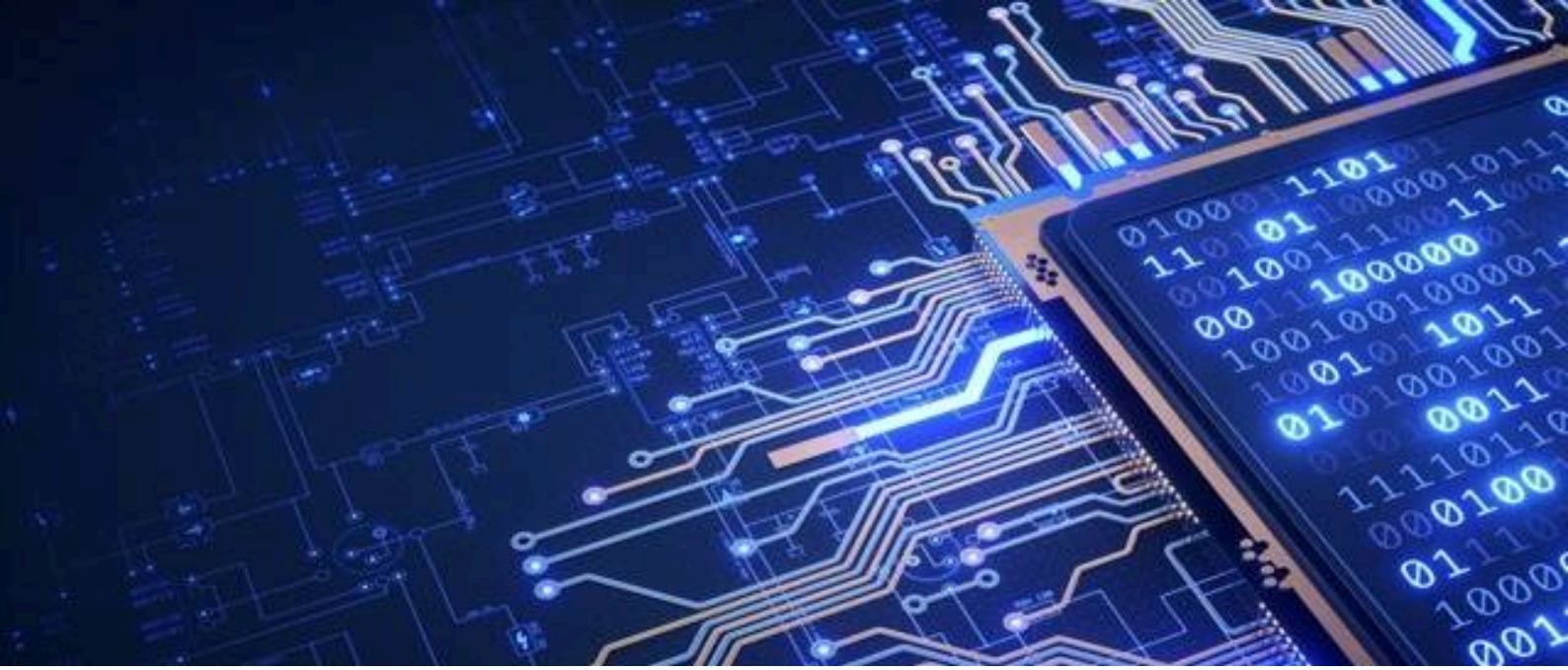

DIGITAL INDUSTRIES SOFTWARE

Aprisa place-and-route tool for low-power SoCs

A place-and-route methodology for lowest-power-optimized performance, power and area

Executive summary

The Aprisa digital design software helps designers address the many challenges of low-power designs. Aprisa is the most flexible IC place-and-route tool on the market—it accepts all industry-standard power formats, has excellent correlation to third-party signoff tools, and is easy to install, set up, and use. With effective technology and impressive usability, the Aprisa software ensures cost-effective tape-outs for power-sensitive designs. This paper introduces the Aprisa low power solution and innovative low-power methodology to quickly converge on low-power-optimized performance, power and area.

Author: Janet Attar

Contents

Low power challenges in place-and-route

Performance, power, and area ("PPA" for short) is a phrase the IC design community commonly uses when describing the three key areas of focus when optimizing an IC design. Traditionally, when talking about PPA metrics, "performance" has been the primary focus. That is, the primary design goal is to achieve performance goals at all costs and then work to recover power and area with minimal effect on timing, or with some small, relatively harmless tradeoff. But as designs have moved to smaller, more advanced process nodes, and as switching activity has become a dominant component in power consumption, power has at times pushed "performance" aside to become the dominant focus in PPA. Of course, designers don't want slower-performing chips, but power consumption is growing in importance.

How can strict power specs be achieved without sacrificing performance during the implementation phase of the IC design process? Many of the challenges of achieving low-power during physical implementation relate to how well the place-and-route software handles multiple power domains and the kind of optimizations the software performs throughout the flow to achieve low power goals.

The place-and-route software used in the digital implementation flow must be able to buffer on multiple power domains without errors and perform placement of all power management cells such as level shifters, isolation cells, power switch cells, and retention flip-flops. Power-sensitive designs also require routing secondary power/ground pins and routing to the power grid inside the voltage islands.

This white paper examines how the Siemens Aprisa place-and-route tool addresses these power challenges in two main ways:

- Through PowerFirst implementation technology that reduces total power consumption

- Through multi-power domain methodology support

But first, a short introduction to the Siemens Aprisa place-and-route solution.

Introduction to the Aprisa digital implementation solution

Aprisa is a best-in-class digital place-and-route software for hierarchical and block-level designs. Aprisa was built from the ground up using modern algorithms to be a detail-route-centric place-and-route tool for fast design closure of hierarchical and block-level designs. By considering the impacts of detail route information throughout the physical design flow, Aprisa can tame the challenges of advanced process node designs, turning complexity into a competitive advantage.

Aprisa uses a unified data model that is shared throughout the entire flow, so there are no data or format conversions between implementation steps. In addition, the unified data model allows real routing information and parasitics to be available to each step in the flow, resulting in consistent timing and DRC and excellent correlation to signoff tools.

Aprisa delivers the best PPA for advanced node designs with patented place-and-route and optimization technologies, ease of use, and complete support for low-power design methodologies which will be presented in more detail in the following sections. Figure 1 illustrates the Aprisa architecture.

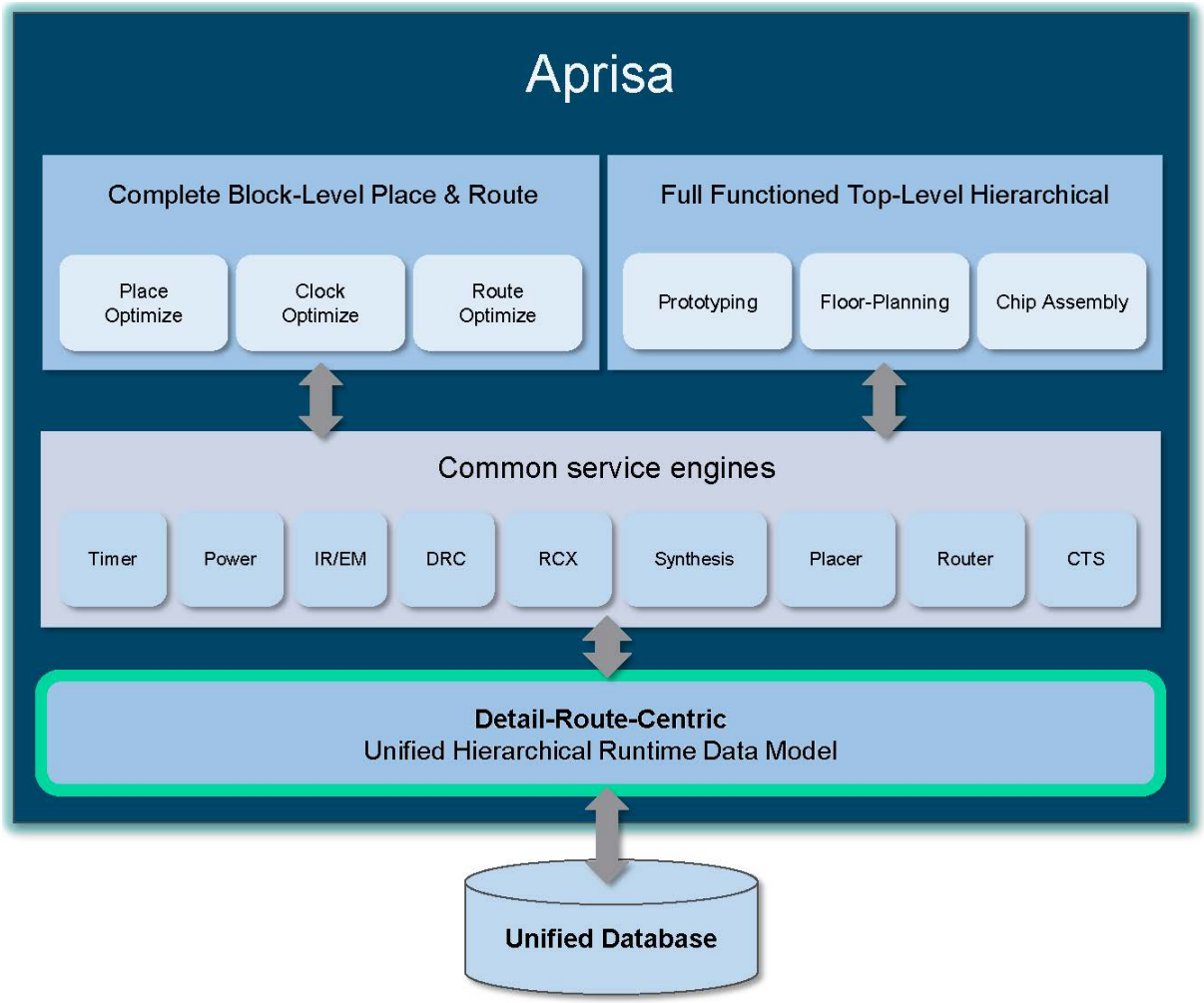

Figure 1. Aprisa architecture for detail-route-centric implementation.

Aprisa low power technologies: PowerFirst

With the design goal of meeting strict power specifications without sacrificing performance, Aprisa PowerFirst optimization takes “best power” as the top priority and works towards that goal throughout the flow, using activity-based placement and routing for lower dynamic power. By starting with the power metric as the top goal during optimization, the place-and-route flow can achieve the best possible power for that node, library, and design specs, and then optimize from that point to reach the timing target (figure 2). This method is more effective than trying to recover power once the most power-hungry cells have already been used in the design to achieve timing.

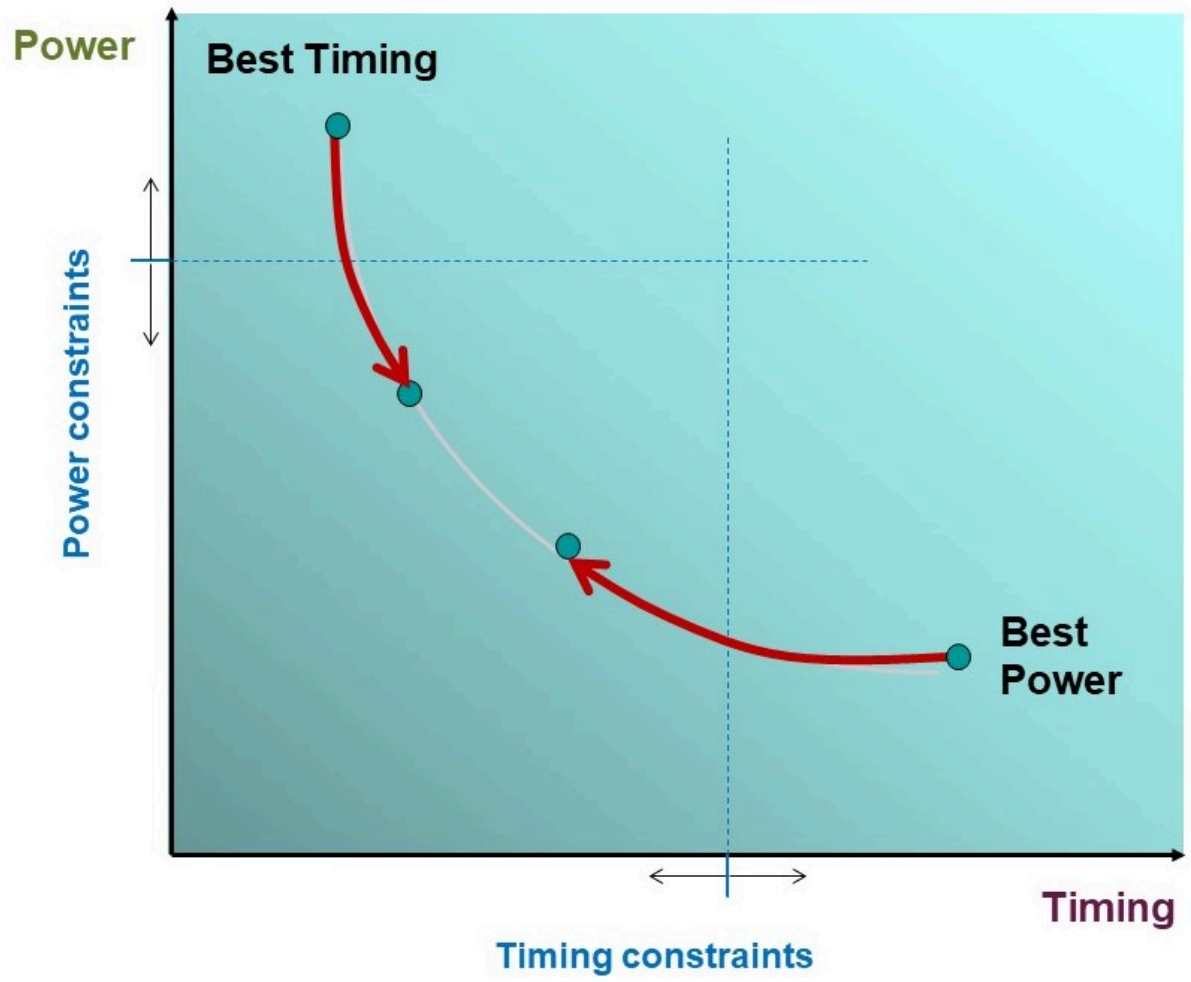

Figure 2. PowerFirst starts from the best power and optimizes to achieve the timing target.

However, designing for power is not just a matter of choosing cells that save power. That's why PowerFirst is considered a methodology, not a single feature; it touches all engines and steps in the flow to ensure power-centric design implementation that can ultimately meet the performance targets for the chip.

Activity-driven methodology for dynamic power

Dynamic power is the dominant concern for high-performance designs. Aprisa uses switching activity throughout the flow to optimize dynamic power.

When the switching activity information is available, all Aprisa engines have access to that information and can use it to make low-power decisions with respect to dynamic power. For example, as seen in figure 3, the placement engine will use the switching information to ensure the high-activity nets have less capacitance compared to the low-activity nets. Aprisa can minimize the net capacitance on those high-activity nets in a number of ways, starting early in the flow. Ensuring power optimization from the start gives better results than using power recovery techniques later in the flow. Similarly, during clock tree synthesis (CTS), Aprisa keeps the high-activity net connections short in the design to reduce capacitance, and the low-activity nets can be spread out to relieve congestion.

The Aprisa router (shown in the last card in figure 3), spaces the high-activity nets to reduce the coupling capacitance and reduce power, but switching activity information allows the router to make decisions about what rules to apply to high- and low-activity nets, as routing resources need to be managed carefully. All the various design engines in Aprisa use the switching activity information, so they can work to reduce power at every stage of the physical design.

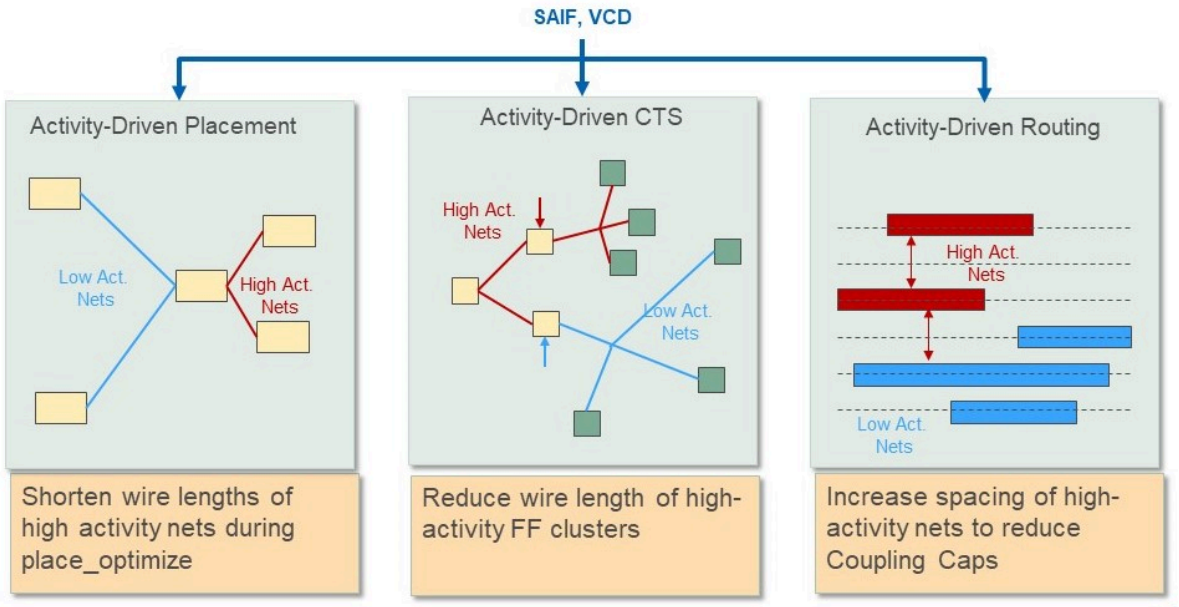

Figure 3. Managing coupling capacitance at various steps helps lower power usage.

Clock transition fixing for better power

Aprisa can reduce switching power by slowing down the sharp transition of the buffers on the clock tree. The goal is to reduce the clock power without violating transition limits. On a timing-only driven design, Aprisa will focus on achieving a sharp transition for most buffers. However, on a power-first design, Aprisa will slow down the transition of many of those buffers without causing transition violations. This technique achieves significantly lower switching power for both cell and nets and in the process can also save area.

Tradeoff small timing for large power reduction in CTS

With the PowerFirst methodology, Aprisa starts early with power vs. timing tradeoffs. When building the clock tree, the typical goal is to achieve the best latency and skew, but this can result in using larger buffers and more of them than what are really needed (figure 4).

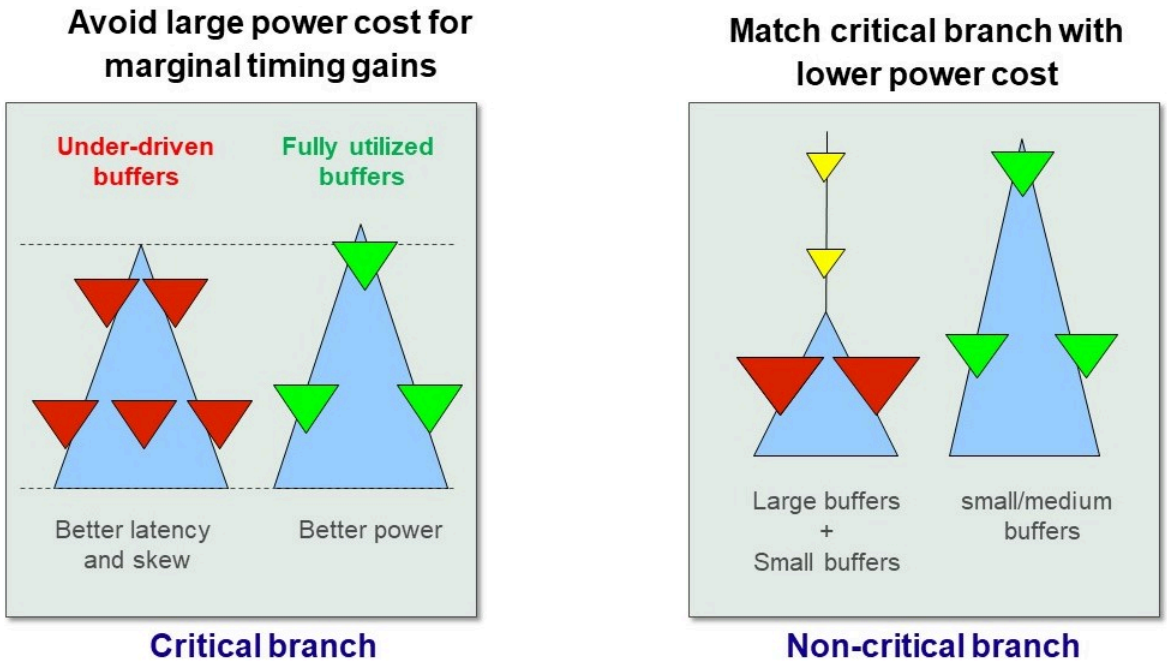

Figure 4. Trade off small timing for large power reduction in CTS.

With a very tight skew, the launch and capture clocks are balanced and the datapath can more easily meet timing. With a larger skew, although the datapath may not initially meet timing, it can be fixed through optimizations like upsizing a cell or adding a buffer. Allowing a larger skew ends up relieving the costs in terms of power that come with a very tight skew, even on the critical branch.

For the non-critical branch, large and smaller buffers are sometimes used in combination to achieve a tight skew. But if the path is not critical, timing is already met, and the tighter skew is not required. This means that a little timing can be sacrificed to reclaim other metrics like power by switching some of the large buffers for smaller ones.

Aprisa looks at the slack value to see if it can cover some of it through datapath optimization; and if that is the case, it can downsize the buffering or remove some buffers altogether in the clock tree. This becomes a good tradeoff between timing and power, and it is a benefit for routing resources and area.

Multi-bit-register merging and de-merging

Another technique, perhaps one of the most popular during physical implementation for reducing dynamic power is using multi-bit flip-flops because they reduce total power by a significant amount.

Aprisa can merge low bit flip-flops into higher bit flip-flops, up to 4- or 8-bit depending on the availability of those cells in the library (figure 5). This reduces dynamic power significantly while the place optimization engine ensures that there is no effect on timing.

During optimization, those paths where the timing potentially degraded due to merging can be de-merged to improve the timing. Aprisa does this dynamically and automatically, achieving a greater number of multi bit flip-flops while maintaining time design closure. The advantage of having Aprisa merge and de-merge during place-and-route rather than performing that operation through logical connection during synthesis for example, is that it can do so within a physical-aware context. It

knows the connections and placement of those multi-bit cells, and it can make merge decisions based on that information, thus achieving timing closure and greater dynamic power reduction.

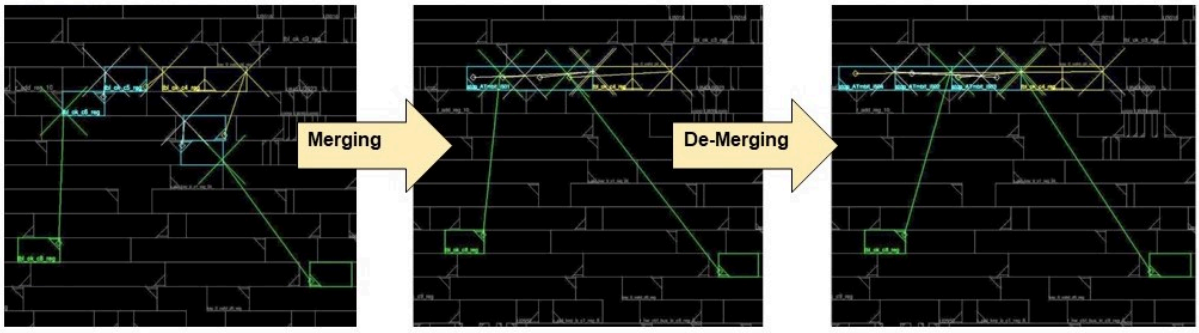

Figure 5. Merging and de-merging multi-bit flip flops.

Full LVF analysis and optimization to reduce over-design

Optimization techniques alone are not enough if the analysis data is not accurate. As technology nodes advanced, on-chip variation (OCV) became increasingly critical to design timing and the industry developed many OCV methodologies to manage the effects. With the introduction of 10 nm and below process nodes, the Liberty Variation Format (LVF) further enhanced the OCV methodology and introduced a table look up for the mean and variants of a gate, according to the input slew and output load.

LVF is the most advanced OCV methodology to date, and it is required by foundries for advanced process nodes. The LVF support is not only needed for signoff STA, but it is also needed during timing optimization. With native and precise support of LVF, Aprisa can avoid unnecessary timing pessimism and avoid over-design, thus improving design PPA.
Aprisa's support of LVF allows accurate optimization for the real failing paths, resulting in better power. Reading LVF natively also means that Aprisa is well correlated with signoff timing, which eliminates unnecessary ECO iterations and improves time to design closure.

Example results from PowerFirst methodology

PowerFirst optimization reduces the internal, switching, and leakage power of the most power-sensitive designs while minimizing timing tradeoffs. In the design shown here, a DDR PHY in 7 nm with about 1.3M instances and a 1 GHz frequency, The customer used Aprisa to optimize total power using the PowerFirst techniques. This includes vector and vectorless activity-driven place and route, timing, placement aware multi-bit register merging and de-merging, and PowerFirst CTS for clock buffer sizing and transition fixing.

The chart in figure 6 shows that using the PowerFirst techniques in Aprisa reduces the total power by 16% compared to Aprisa in timing-only mode while maintaining the achieved timing correlated to signoff. The results from a competitor's place-and-route tool in power savings mode did not achieve the same level of total power reduction as Aprisa.

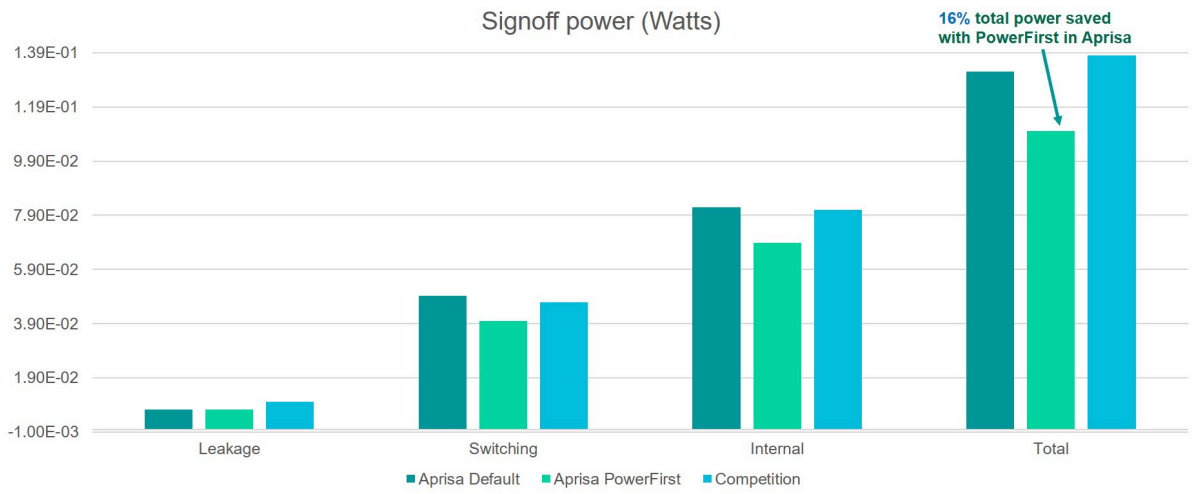

Figure 6. Results of Aprisa PowerFirst on internal, switching, and leakage power at sign-off.

Aprisa low power technologies: multiple power domain support

While PowerFirst techniques work directly to reduce dynamic and leakage power, multi-power domain support ensures all the elements required in a low power design are included and used in accordance with the low-power specs.

Aprisa has comprehensive multi-power domain support, and it supports UPF. UPF contains the power intent and unique functions specific to multi-voltage designs. This can determine what power management cells should be implemented in the design.

Aprisa can do automatic insertion of power management cells, such as isolation cells, level shifters, power switches, always-on/regular buffer selection.

Its unique Power Domain Checker can flag the errors related to power domain, cell placement, connectivity, and buffering. Figure 7 illustrates power state table representation of power intent.

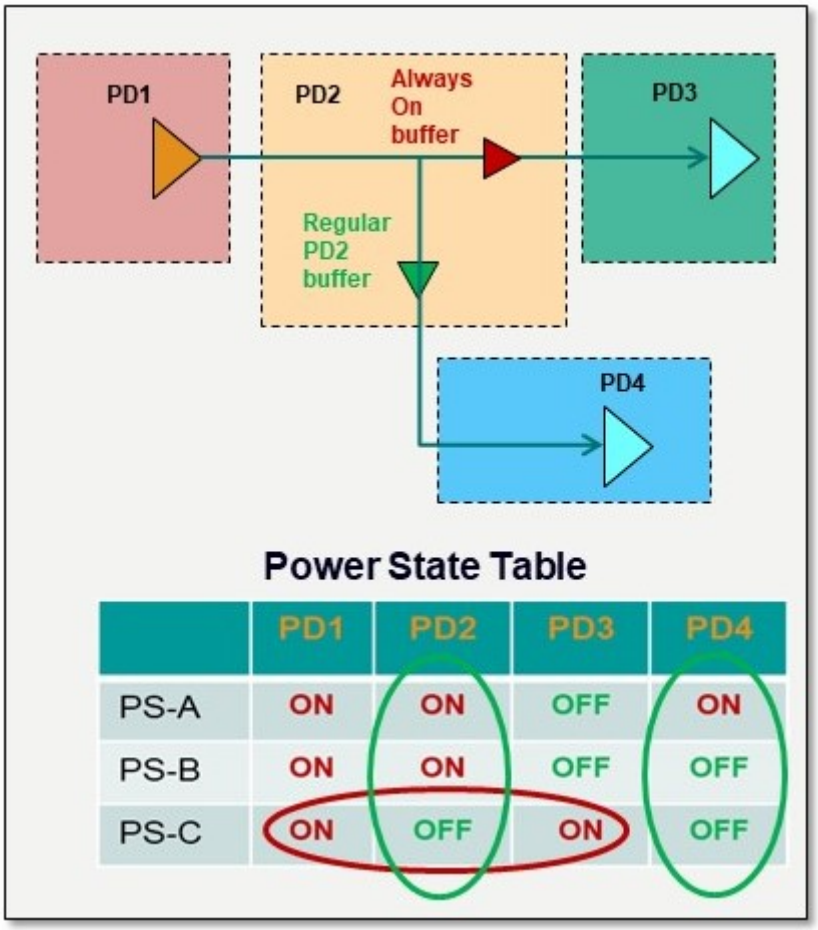

Figure 7. Power state table representation of power intent.

Power switches

Power switch rules can be defined with UPF to indicate where they are needed and how they should be connected. Typically, power switches connect one or more input supply nets to a single output supply net based on control inputs.

There are two types of connections: a header cell and a footer cell. The header cell (which is the most common) switches the power supply. A footer cell switches ground supply. Power switches may be inserted around the perimeter of the power domain or distributed throughout the domain, as shown in the two pictures in figure 8.

Aprisa can insert power switches and place them in rows, columns, arrays, rings, or checkerboard patterns (around or over a block), and it can daisy-chain the enable pins.

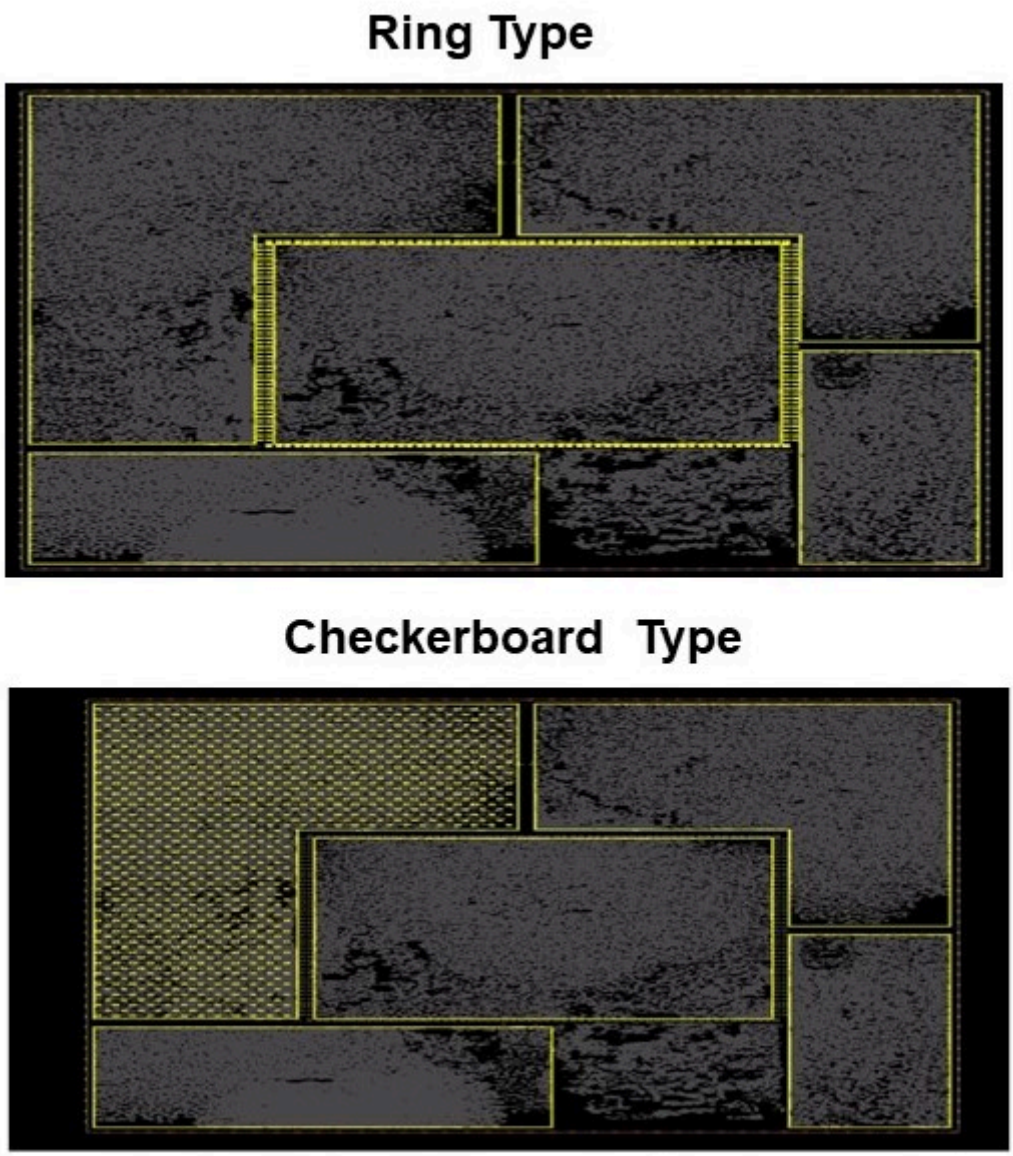

Figure 8. Power switch placement options.

Always-on Buffering in Multi-voltage Designs

Aprisa has two main methodologies for always-on-buffer support: Always on buffer cells and voltage islands.

Always on buffers are repeaters powered by a supply different from the power domain supply where they are located. They therefore require a secondary PG pin to connect to that alternate supply. When these repeaters are available in the library, Aprisa can insert them and handle the routing of that secondary PG pin to the alternate power supply.

The second method uses power islands or voltage islands that are created to the specs of the design. Aprisa places regular repeaters on those islands, which are connected to a grid of a different power supply. The images in figure 9, show the different methodologies of using an always-on cell (left), and of using a regular repeater inside a voltage or power island (right).

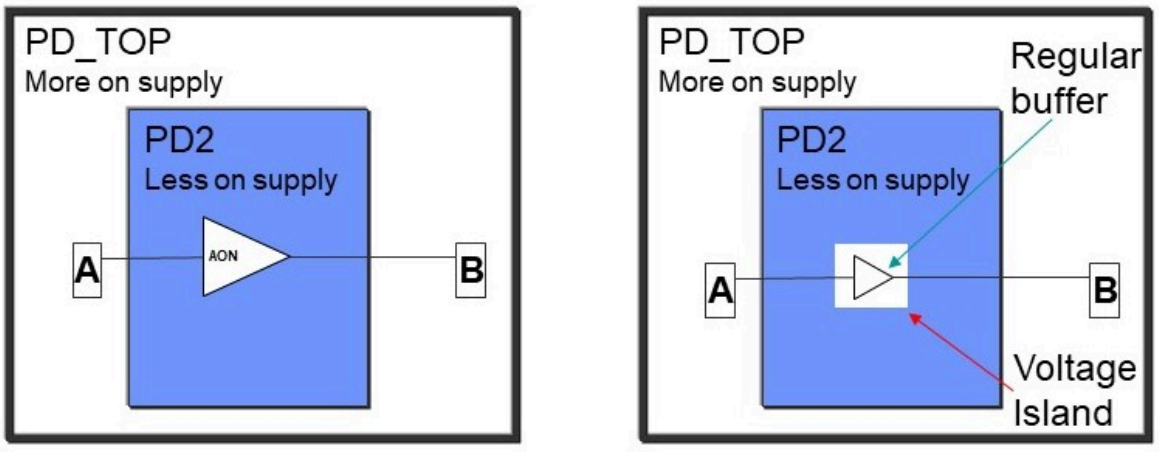

Figure 9. Always-on cell vs. voltage island.

Connection to supply always-on buffers

Multi-power domain designs pose specific challenges to place-and-route tools when it comes to routing. While designers must weigh the advantages and disadvantages of using always-on buffers (AON) vs voltage islands, both require careful management when it comes to routing. Aprisa helps designers ease those challenges no matter what technique is chosen by extending the capabilities of its patented sibling routing technology for use on power signals and regular signals from repeaters used within voltage islands.

In the case of AON cells, as shown on the left side of figure 10, Aprisa can automatically connect the tie signal to the nearest always-on rail. Using these repeaters gives the flexibility of placing them exactly where needed, but if the connection to the alternate supply is long, this could lead to IR drop issues.

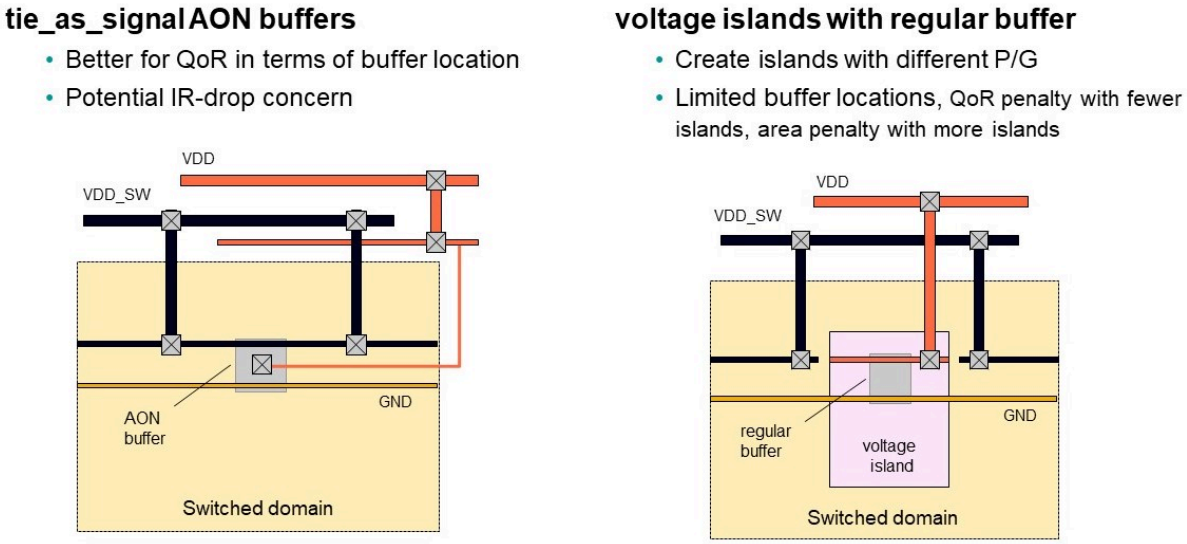

Figure 10. Connection to supply always-on buffers.

To reduce such issues, sibling via pillars are used to route the AON repeater's secondary PG pin to the always-on supply as shown in figure 11 (left). This technique produces a cleaner routing topology (right), thus reducing IR drop issues.

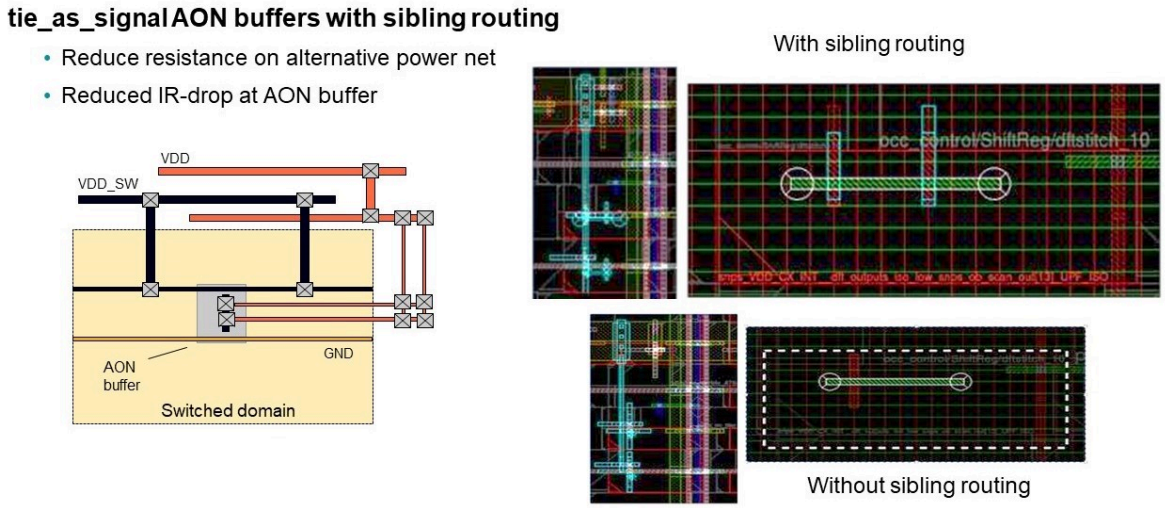

Figure 11. Sibling routing technology for alternative power supply.

When using voltage islands (figure 10, right), the island itself has a different supply and regular repeaters can be used in this case. There is a tradeoff between how many of these islands to add to the design, and how far to spread them out. Too many, and there is an area, congestion, and routing penalties; too few and there may be timing issues on the buffer are placed to resolve a timing issue to begin with. Furthermore, if the islands are too sparse it can lead to buffers not being placed in an optimal location.

Aprisa can use sibling routing technology to connect the pins of those repeaters creating the via pillars on the fly without the designer having to manually intervene. Sibling routing is able to access the lower layer metal pins with a parallel wire structure only available with the Aprisa router. It uses "parallel wires" to connect to the pins as well as to vias up to the higher layers. Sibling wires are automatically created during route optimization only on those nets that need it. However, designers have the flexibility to create them with NDR-like rules called sibling route rules. Sibling routing reduces resistance, which helps with electromigration (EM) and improves timing.

Sibling routing and secondary PG pins

As previously discussed, IR drop on secondary PG nets is a big concern, and it impacts the performance of the always-on cells. Aprisa can use sibling route to reduce resistance on those secondary PG nets. Figure 12 (left) shows the secondary PG pins routed in the traditional manner, and the resistance of the secondary power net is 242 Ohms. With sibling route (right), resistance is reduced significantly to 128 Ohms.

Figure 12. Resistance on secondary power nets with regular routing vs. sibling routing.

A unique strength of Aprisa is that it can do resistance-aware secondary PG routing, which can result in optimal use of routing resources. Aprisa can dynamically decide where to place sibling routes to use them only as required to conserve those routing resources.

To recap, sibling routing technology is intended to create the shortest possible connection to ensure the least resistance: (1) by sharing of fanout to use optimal routing resources; (2) with NDRs and sibling rules that can be applied on lib pins; and (3) the extension of this patented technology can be used to route secondary PG pins to reduce IR drop when using always-on buffers.

Built-in Power Domain Checker

Aprisa offers a comprehensive power domain checker within the tool that checks multi-voltage setup, power management cells, and correct connectivity. A view of the power domain checker is shown in figure 13.

```
SUMMARY:
        WARNING:     23  nets with multiple drivers from different supply/domain.
        ERROR   :    511  nets without proper isolation/level_shift.
        WARNING:     53  isolation-cells/level-shifter may not be needed (same supply).
        WARNING:     23  isolation-cells/level-shifter may not be needed (no sink).
        WARNING:      8  isolation cells/level-shifter with no matching rule.
        ERROR:       10  isolation-cell/level-shifter lib_cell.
        WARNING:    242  power-switch cell enable pin disconnected.
        WARNING:     11  PowerState supply does not belong to any power domain.

[From supply     :To supply       ] Need         #ISO/LS   iso/ls-rules
-------------------------------------------------------------------------------
[VDD_VESD        :VDD_BOOSTV33    ] --------HL   =     0
[VDD_VESD        :VDD_V11BKPRAM   ] --------HL   =     0   LSV_V33T0V11BKP
[VDD_VESD        :VDD_V11         ] --------HL   =     0   LSV_V33T0V11EXT
[VDD_VESD        :VDD_V110        ] --------HL   =     0   LSV_G02_T0_V110
[VDD_VESD        :VDD_V11I        ] --------HL   =     0   LSV_G02_T0_V11I ...
[VDD_V33SW       :VDD_BOOSTV33    ] --------HL   =     0
[VDD_V33SW       :VDD_V11BKPRAM   ] --------HL   =     0   LSV_V33T0V11BKP
[VDD_V33SW       :VDD_V11         ] --------HL   =     0   LSV_V33T0V11EXT
[VDD_V33SW       :VDD_V110        ] --------HL   =     1   LSV_G02_T0_V110
[VDD_V33SW       :VDD_V11I        ] --------HL   =     1   LSV_G02_T0_V11I ...
[VDD_VSWESDINV33 :VDD_BOOSTV33    ] --------HL   =     0   LSV_G01_V33_T0_VSW ...
[VDD_VSWESDINV33 :VDD_V11BKPRAM   ] --------HL   =     2   LSV_G01_V33_T0_VSW ...
[VDD_VSWESDINV33 :VDD_V11         ] --------HL   =     0   LSV_G01_V33_T0_VSW ...
[VDD_VSWESDINV33 :VDD_V110        ] --------HL   =   256   LSV_G01_V33_T0_VSW ...
[VDD_VSWESDINV33 :VDD_V11I        ] --------HL   =    52   LSV_G01_V33_T0_VSW ...
[VDD_VBAT        :VDD_BOOSTV33    ] --------HL   =     0
[VDD_VBAT        :VDD_V11BKPRAM   ] --------HL   =     0   LSV_V33T0V11BKP
[VDD_VBAT        :VDD_V11         ] --------HL   =     0   LSV_V33T0V11EXT
[VDD_VBAT        :VDD_V110        ] --------HL   =     0   LSV_G02_T0_V110
[VDD_VBAT        :VDD_V11I        ] --------HL   =     0   LSV_G02_T0_V11I ...
[VDD_V33         :VDD_VESD        ] isox------   =     0
[VDD_V33         :VDD_V33SW       ] isox------   =     0
[VDD_V33         :VDD_VSWESDINV33 ] iso0------   =    17   ISOLV11IVSWA ...
[VDD_V33         :VDD_VBAT        ] isox------   =     0
[VDD_V33         :VDD_BOOSTV33    ] --------HL   =     0   LSV_G01_T0_V33 ...
[VDD_V33         :VDD_V11BKPRAM   ] --------HL   =     0   LSV_G01_T0_V33 ...
[VDD_V33         :VDD_V11         ] --------HL   =     4   LSV_G01_T0_V33 ...
[VDD_V33         :VDD_V110        ] --------HL   =    51   LSV_G01_T0_V33 ...
[VDD_V33         :VDD_V11I        ] --------HL   =    57   LSV_G01_T0_V33 ...
[VDD_V33SD       :VDD_VESD        ] isox------   =     0
[VDD_V33SD       :VDD_V33SW       ] isox------   =     0
[VDD_V33SD       :VDD_VSWESDINV33 ] iso0------   =     0   ISOLV11IVSWA ...
[VDD_V33SD       :VDD_VBAT        ] isox------   =     0
[VDD_V33SD       :VDD_BOOSTV33    ] --------HL   =     0
[VDD_V33SD       :VDD_V11BKPRAM   ] --------HL   =     0   LSV_V33T0V11BKP
```

Figure 13. Built-in Power Domain Checker.

Aprisa's checker can identify all the power domain-related errors without the need of an external verification tool and long before going to signoff, which can ensure correct-by-design low-power methodology and use of power management cells as required.

In general, most power management cells will already be inserted on the synthesized netlist, and Aprisa's power domain checker can catch any missing or incorrect cells. If missing, Aprisa can insert those power management cells, such as level shifters and isolation cells, and then do optimization. It can also provide information after optimization to ensure there are no errors in a way that is easy and intuitive to use and review. Having the checker integrated allows the designer to do follow-up checks after other optimization steps, keeping tabs on any errors that may have occurred at any step.

Having this information during P&R can help designers fix any issues while routing resources, congestion and timing are still manageable. This also allows for an accurate picture of PPA metrics, and helps keep close correlations with signoff tools, which can avoid costly ECOs.

Conclusion

Design teams will always strive to achieve the best possible PPA. As process technologies introduce greater challenges to power and as more applications strive for better power management, having tools and new methodologies to better manage power has become ever more essential. The Siemens team has put a lot of thought and ingenuity into helping implementation teams converge on the best PPA possible. To learn more, visit the Aprisa web page.

Siemens Digital Industries Software

Offices

Headquarters
Granite Park One 5800 Granite Parkway
Suite 600
Plano, TX 75024 USA
+1 972 987 3000

Americas
Granite Park One 5800 Granite Parkway
Suite 600
Plano, TX 75024 USA
+1 314 264 8499

Europe
Stephenson House
Sir William Siemens Square Frimley, Camberley
Surrey, GU16 8QD
+44 (0) 1276 413200

Asia-Pacific
Unit 901-902, 9/F
Tower B, Manulife Financial Centre
223-231 Wai Yip Street, Kwun Tong
Kowloon, Hong Kong
+852 2230 3333

For additional numbers, click here.

About us

Siemens Digital Industries Software helps organizations of all sizes digitally transform using software, hardware and services from the Siemens Xcelerator business platform. Siemens' software and the comprehensive digital twin enable companies to optimize their design, engineering and manufacturing processes to turn today's ideas into the sustainable products of the future. From chips to entire systems, from product to process, across all industries. Siemens Digital Industries Software – Accelerating transformation.

Janet Attar

10/2023